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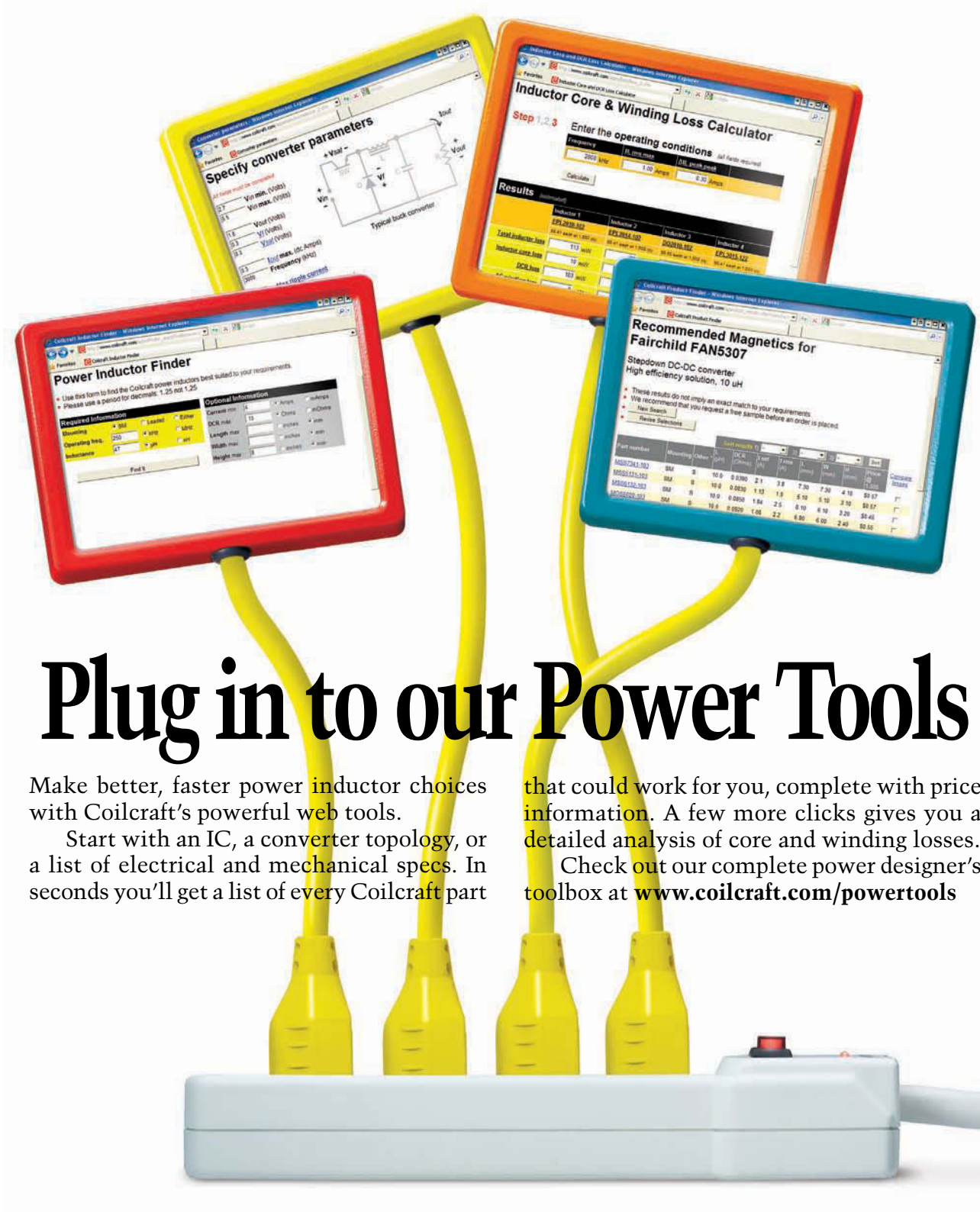

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By Harry Holt, Analog Devices Inc

pulse

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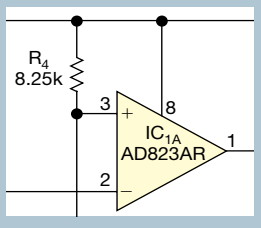

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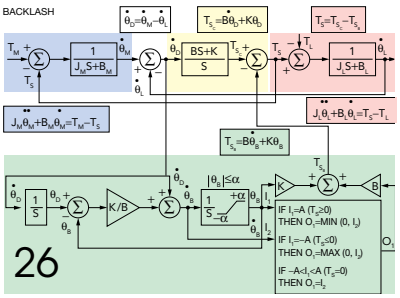

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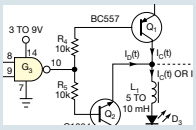

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Volume 56, Number 16 (Printed in USA).

BY PAUL RAKO, TECHNICAL EDITOR

Those crazy engineers

Once a Gila monster bites its prey, it never lets go until the prey is dead. Engineers should do the same to problems—perhaps not every problem, but now and then pick a battle and just don't let go until you figure it out. It may seem a waste of time to those around you, especially your boss or your spouse. Yet persistence in solving problems makes you a better engineer and gives you a deeper understanding of what you are working on. Better yet, it gives you a better understanding of how to solve problems. By developing a reputation as a tenacious problem solver, you will become the go-to guy when something serious comes up. That reputation will surely help your career because management will see that you do the tough jobs.

I first saw what I considered crazy behavior in a consultant pal. My friend John Haggis is a software programmer, but he understands and respects hardware. Around 1985, like many of us, Haggis was building his own PC, but the add-in cards he had implemented just wouldn't work. Back in the DOS days, you had to set a little DIP switch on the add-in card to select an interrupt line. Haggis had several add-in cards in the PC he was building. He had spent days trying to get all the cards to work properly. He didn't let his title of programmer stop him from dragging out an oscilloscope and looking at the interrupt signals. He soon saw that the only way to make all the cards work was to assign a certain interrupt line to one of them. That card had no edge-card-connector pin for the interrupt.

Although most engineers might have given up, Haggis instead found an add-in card in a different slot that had an unused connector pin. No trace connected to the pin, so he knew the card didn't need that particular interrupt. He took some blue wire-wrap wire and connected the problem add-in card DIP switch to the edge-card connector pin on the card next to it. All the add-in cards then finally worked properly.

By marching up the ramparts of a problem, you learn the details of how something works.

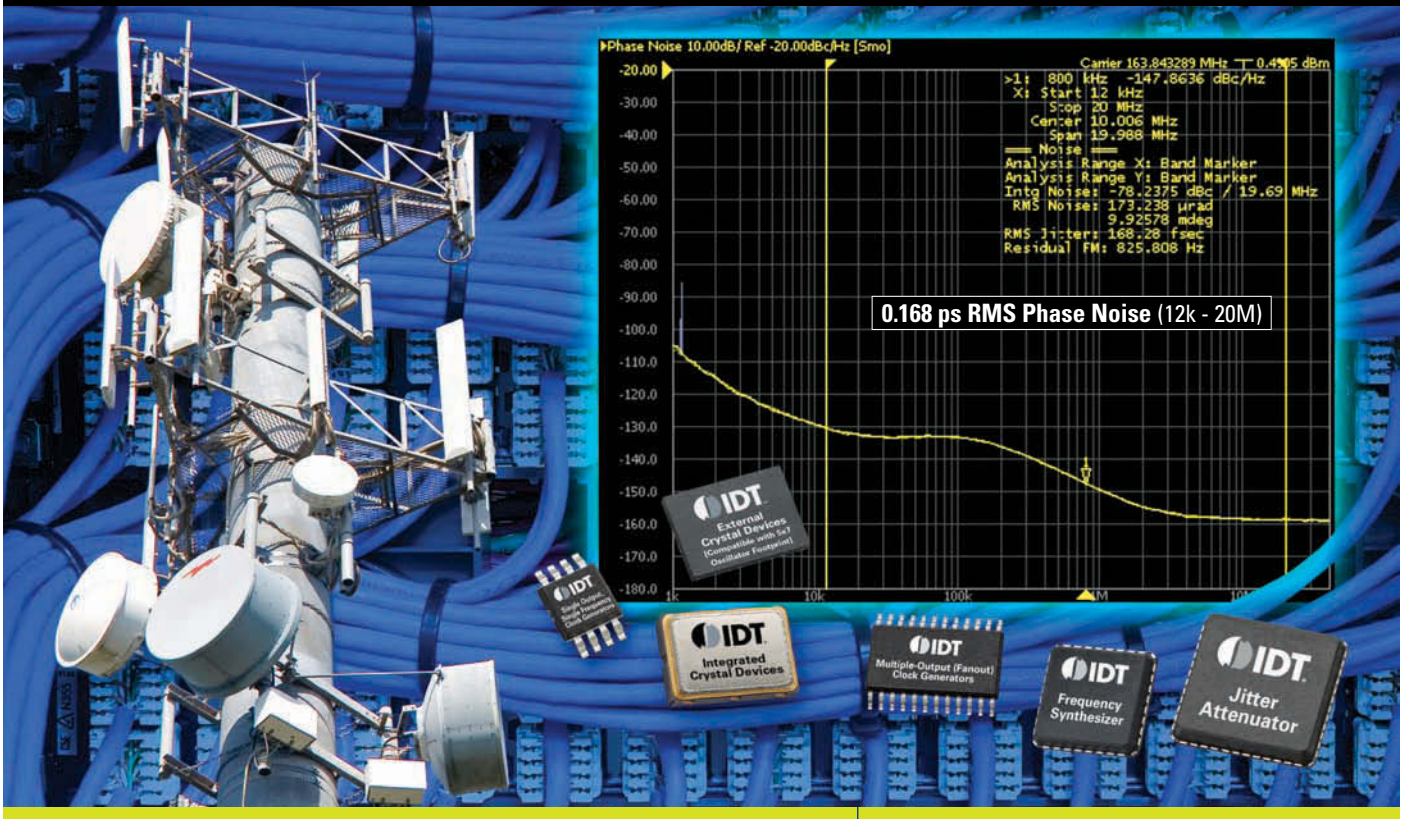
In 2004, I worked with Paul Grohe at National Semiconductor. Grohe was trying to put one of those old problematic Turtle Beach sound cards into an even older Windows 95 PC. Like Haggis, Grohe had no fear of seemingly unsolvable problems. Over daily weekday lunches in National's cafeteria, several other engineers and I became more critical of Grohe's seemingly absurd fixation with this problem. We told him to toss out the Turtle Beach card; everyone knew it was a problem. We told him to upgrade the OS to Windows 98 or Windows XP. We told him he could throw the whole computer in the garbage and get a new one for much less than the cost of the time he was spending to solve this problem.

Nevertheless, Grohe soldiered on. "It's not going to beat me; I will get this working," he told us. It took him two weeks, but, one day, he came in all smiles. He had searched news groups. He had read documentation. He had learned how to update everything from the BIOS to the video drivers. Two weeks later, he upgraded the computer to Windows 98, and it seemed as if he had just thrown away all that work. Sure, knowing the details of a sound-card installation on an obsolete operating system might seem insignificant. But learning how a PC, the operating system, and those same pesky interrupts worked gave Grohe a foundation for solving modern-PC problems, as well.

With tenacity, by marching up the ramparts of a problem after all around you have fallen, you learn the subtle details of how something works. You also learn the simplest and fastest way to take on what others considered an unsolvable problem. Haggis and Grohe are exceptional engineers, and, when I have a tough problem, they are on my short list of people to call to get insight and a method for solving it. We should all try to have the same level of tenacity. At first your boss might resent your spending so much time on a problem. As you get better at finding solutions, though, your boss will come to cherish your contribution, just as I cherish my crazy engineer friends. EDN

Contact me at paul.rako@ubm.com.

Integrated D evice Technology FemtoClock NG – When a Trillionth Of a Second is Just Too Long



The FemtoClock Next Generation (NG) clock synthesiser family allows engineers to generate almost any output frequency from a fixed frequency crystal, and to meet the challenges of the most demanding timing applications.

Use of a single source to generate multiple clocks often leads to increased susceptibility to power supply noise and restrictions on multiplication factors. IDT's technology effectively eliminates these problems by doubling the power-supply noise rejection (PSNR) of previous generation devices while also introducing the potential for virtually limitless customization of output frequency.

An innovative fractional multiplier PLL architecture introduces the flexibility for engineers to generate any output frequency from any input frequency. And the advanced design of the FemtoClock NG family achieves greater than 80 dB of PSNR to make the devices immune to power-supply noise.

Other performance benefits of FemtoClock NG technology include low power consumption and a clocking performance of under 0.5 ps RMS phase noise jitter! The devices offer standard outputs such as differential LVPECL, LVDS and single-ended LVCMOS, providing a precise fit to any application.

With FemtoClock NG technology, IDT has eliminated the most challenging aspects of silicon-based clock design and introduced an unprecedented level of flexibility for clocking in high-performance applications.

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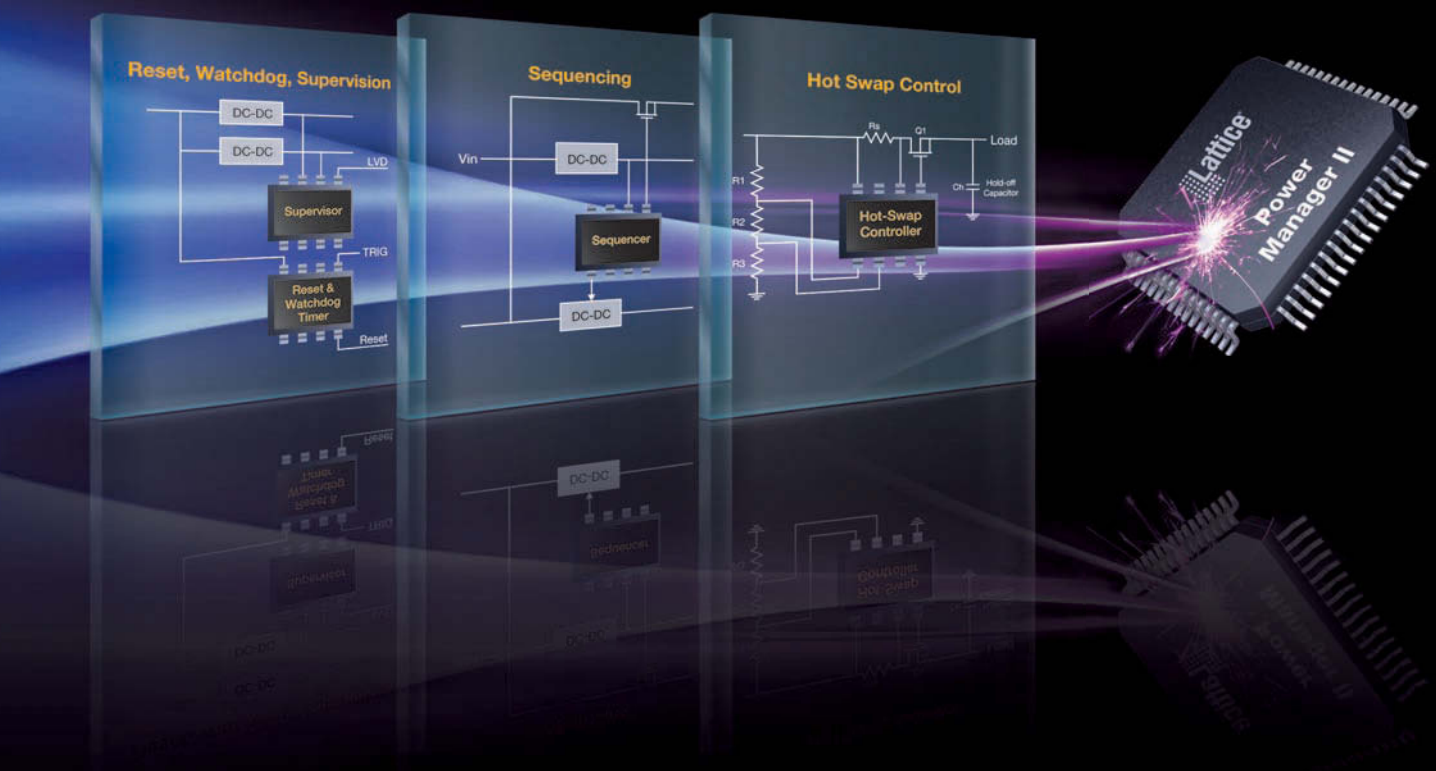

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Low-power audio codec prevents speaker damage

Maxim's new MAX98089 stereo audio codec improves audio performance, prevents speaker damage, and includes an easy-to-use GUI (graphical user interface). To minimize the number of discrete components, the device integrates jack detection, which detects button presses and the insertion and removal of accessories. DAC-to-headphone idle power consumption is 5.6 mW, extending battery life. The device targets use in portable-multimedia applications, including tablets, netbooks, and mobile phones.

The MAX98089 features the company's proprietary FlexSound audio technology, which enhances the signal level, improves the frequency level, and limits the maximum distortion and power at the output. This technology improves loudspeaker performance and prevents speaker damage. FlexSound comes with an extensive tool kit for improving loudspeaker-playback performance and voice transmission.

The GUI lets you evaluate and optimize the MAX98089's five-band parametric equalizer, automatic level control, speaker-excursion limiter, speaker-power limiter, and speaker THD (total harmonic distortion) limiter. Software drivers are available for Linux and other OS platforms. Automatic gain control and a noise gate optimize the signal level of the microphone's input signals.

The device also integrates a Class H stereo-headphone amplifier with a dual-mode charge pump, eliminating the need for output capacitors and ensuring click- and pop-free operation during turn-on, turn-off, and volume changes. Ground sense reduces the output noise that ground-return current causes. Low-EMI (electromagnetic-interference), stereo, Class D speaker amplifiers provide filterless operation in the amplification of two speakers.

The MAX98089 comes in a 3.8×3.3×0.4-mm pitch, 63-bump WLP or a 7×7-mm, 56-pin TQFN and operates in the extended-temperature range of –40 to +85°C. Prices start at $1.98 (1000). **—by Fran Granville**

▷**Maxim Integrated Products**, www.maxim-ic.com/mobility.

TALKBACK

"We are getting exactly what the school system was designed to produce—a uniformly dumbed-down product of compliant, lackluster people who have had their individuality crushed out of them by a system that rewards mediocrity."

—Aerospace engineer John Ross, in *EDN*'s Talkback section, at http://bit.ly/nHMMIm. Add your comments.

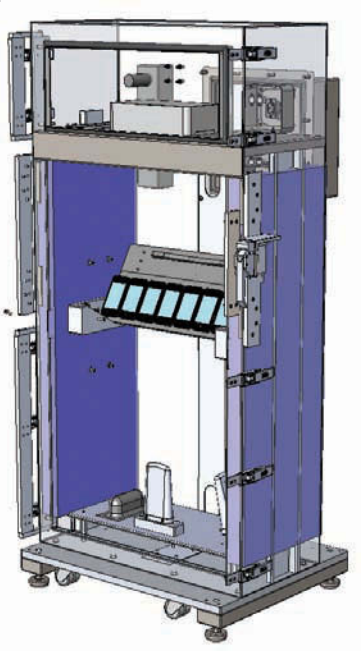
The easy-to-use MAX98089 audio codec reduces power and boosts audio fidelity.

Smartphone test platform comes in reduced footprint

OctoScope has developed a test system that it claims revolutionizes the design, testing, and verification of multiradio devices, such as smartphones, PC clients, base stations, and USB (Universal Serial Bus) dongles. The octoBox provides accurate OTA (over-the-air) testing of conventional and MIMO (multiple-input/multiple-output) wireless devices in a customizable refrigerator-sized anechoic enclosure.

An OTA test setup must couple a 3-D electromagnetic-energy field into the test instrumentation, which is considerably more challenging to do in a controlled and repeatable manner. A single unit enables simultaneous parallel testing of eight or more fully assembled smartphones through their antennas. It also enables seamless RF-technology validation during development cycles and production and provides stable far-field conditions with advantages for OTA-measurement accuracy, sensitivity, and repeatability.

The system's dual-chamber architecture allows test instrumentation and the DUT (device under test) to reside in the same enclosure, as a self-contained test station with isolation from the interference of neighboring stations. In addition to measuring a DUT's 3-D antenna pattern, octoBox can integrate test equipment, including a MIMO-channel emulator, interference generators, RF sensors, data monitors, and other instruments. It supports a frequency range of 700 MHz to 6 GHz and finds use in testing multiradio smartphones, with 3G (third-generation), 4G (fourth-generation), Wi-Fi, Bluetooth, and GPS (global-positioning-system) radios, all operating in different regions of the spectrum.



The octoBox provides accurate OTA testing of conventional and MIMO wireless devices in a customizable refrigerator-sized anechoic enclosure.

The top chamber of the octoBox typically houses test equipment or a partner device transmitting to and receiving from the DUT. The DUT chamber houses the DUT and the test antennas and features far-field coupling and a uniform antenna field between the DUT antennas and the test antennas.

Optimizing the octoBox for the antenna patterns of each DUT is a natural extension of octoScope's RF- and wireless-consulting services. The octoBox sells for $29,800.

—by Colin Holland

▷**OctoScope**, http://octoscope.com.

NI updates LabView with improved hardware integration

National Instruments recently unveiled NI LabView 2011, the updated version of its design software. The company is celebrating the 25th anniversary of the system-design software with new engineering-specific libraries and the ability to interact with almost any hardware device or deployment target, including the multicore NI CompactRIO controller and the NI PXIe-(Peripheral Component Interconnect extensions for instrumentation)-5665 RF vector signal analyzers. It also supports assemblies built in the latest Microsoft .NET (www.microsoft.com) Framework and includes user-feedback-driven features.

"We created LabView to help engineers focus on innovating instead of wrestling with complicated programming and system-integration issues," says LabView inventor Jeff Kodosky, National Instruments' co-founder and business and technology fellow. "Today, it has become the ultimate system-design software for measurement and control. With each new version, whether by ensuring integration with the latest hardware, introducing new libraries and APIs [application-programming interfaces], or implementing engineer-requested features, our primary objective remains to increase productivity in any engineering situation."

National Instruments based LabView on a structured data flow. The inherent parallelism of data flow was a natural fit for the acquisition-analysis-presentation problems the company's customers were solving. "When the industry moved to multicore machines, that decision made us look downright prescient," says Kodosky.

—by Colin Holland

▷**National Instruments**, www.ni.com.

DILBERT By Scott Adams

RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Balancing Phase in High-Speed Converters

Q. Why is analog input phase balance so important to my high-speed converter design?

A. Analog input phase balance is critical throughout the signal chain, because without proper balance, second-harmonic and other even-order distortion will arise. Analog input phase imbalance typically results when component tolerances or symmetric PCB layout are ignored during the design process.

Phase imbalance occurs when the two differential analog input signals sampled by the A/D converter are not exactly 180° out of phase. In the simplest case, the signals can be thought of as two sine waves. As these two sine waves move apart from "perfect" phase, distortion results. The distortion increases as the system frequency increases, with even-order distortion degrading even quicker.

Passive imbalance, caused by using a transformer or balun to couple the signal to the converter's analog inputs, generally begins around 100 MHz to 150 MHz with standard ferrites. Using two transformers or baluns can reduce the coupling differences and improve the phase balance. Unfortunately, transformers are large and expensive, so using two increases the board space and system cost. The other solution is to use a better transformer.

Active imbalance, caused by using an amplifier to drive the converter's analog inputs, generally happens if component tolerances are not adequate. To minimize beta variation, resistors with 1% or better tolerance should be used for setting the gain. Mismatch will cause the voltages on the summing nodes to differ slightly, resulting in errors on the amplifier's differential outputs and giving rise to second order distortion.

Layout imbalance is caused by asymmetrical traces throughout the signal chain, with a sloppy layout causing decreased system performance. Second-order distortion can arise from asymmetrical connection to the differential input pins of the converter. This may not manifest itself at low frequencies, but nonlinearities will usually show up at frequencies above 100 MHz, so don't throw away your hard work; guide the CAD engineer to keep the front-end design symmetrical and well balanced.

ADC imbalance is caused by a mismatch in phase. The converter can tolerate a certain degree (pun intended) of phase mismatch, but keeping it to 4° or less will yield the best performance. The converter has some inherent imbalance, but designers work hard to keep the IC well balanced internally.

To Learn More About Input Phase Balance
http://dn.hotims.com/34940-100

Contributing Writer Rob Reeder is a senior converter applications engineer working in Analog Devices high-speed converter group in Greensboro, NC since 1998. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, IL in 1998 and 1996 respectively. In his spare time he enjoys mixing music, art, and playing basketball with his two boys.

Have a question involving a perplexing or unusual analog problem? Submit your question to: www.analog.com/askRob

For Analog Devices' Technical Support, Call 800-AnalogD

Localized haptics grabs handheld-game displays with new driver chip

Electronic devices generally depend on visual and audio cues for communications with users, relegating touch to the "dumb buzz" that cell phones use to get our attention when in silent mode. Yet, touch can be a fast, effective communication channel; at the simplest level, it serves as a confirmation that a user has pushed a button or a switch. At the most sophisticated level—gaming devices—tactile feedback can add a whole new dimension of interactivity and go a step closer toward mimicking the real-world experience.

Haptics technology, encompassing devices that interface with the user through the sense of touch, exploits this new dimension. Texas Instruments, for example, recently demonstrated a haptics-based smartphone-guitar game whose screen has different localized vibrational feedback for different fret positions on each string.

The DRV8662 piezoelectric-haptics-driver IC features an integrated 105V boost converter, a power diode, and a 50 to 200V p-p, fully differential amplifier that operates from a 3 to 5.5V supply voltage. The chip requires no external transformer.

You can't do this type of haptics with the old-style ERM (eccentric-rotating-mass) motor or LRA (linear resonant actuator). These technologies work fine for the old dumb buzz, but localized haptics require piezoelectric actuators, which deform when you apply a voltage. The less-than-1-mm-thick devices have start-up times of 1.5 msec and a frequency-generation range of 0 to 300 Hz. Single-layer devices have lower capacitance, require less drive current, and are less expensive, but they require as much as 200V of drive voltage. Multilayer actuators have a higher capacitance, require a higher drive current, have only an approximately 50V drive voltage, and are more expensive.

Entering the haptics field, Texas Instruments recently introduced the DRV8662 piezoelectric-haptics-driver IC, which integrates a 105V boost converter and features a power diode and a 50 to 200V p-p, fully differential amplifier that operates on a 3 to 5.5V supply voltage. It can operate directly from a battery and requires no external transformer. The company claims that the transformerless design is 40% cheaper and takes up only half the board space of competing designs.

Piezoelectric modules' fast start-up, thin form factor, and high bandwidth enable the production of haptic effects that are not possible with inertial-based actuators. The IC drives piezoelectric-actuator capacitances of 50 to 680 nF at 300 Hz, enabling high-resolution haptic effects, including feedback localized to specific areas of the device and vibrations and pulses that change in frequency depending on how the user is interacting with the device. Thermal-overload protection prevents damage when a user overdrives the device, which comes in a 4×4×0.9-mm QFN package and sells for $1.75 (1000).

—by Margery Conner

▷**Texas Instruments**, www.ti.com.

Cree shows off its proof-of-concept 152 lumens/W LED bulb

Cree is showing off a proof-of-concept LED bulb that delivers more than 1330 lumens and consumes 8.7W for an efficacy of 152 lumens/W. The lamp uses Cree's TrueWhite technology to achieve a CRI (color-rendering index) of 91 at a warm-white color of 2800K. As a comparison, a traditional 75W incandescent light bulb delivers 1100 lumens for an efficacy of only 14.6 lumens/W.

Cree claims that the bulb beats the performance requirement for the Department of Energy's L Prize competition in its third category, the 21st Century Lamp. The only criteria that the DOE has so far released for this category are that the lamp must exceed 150 lumens/W and must meet the general criteria of the L Prize lamps of producing 1200 lumens, at least 150 lumens/W, a greater-than-90 CRI, and 2700 to 3000K CCT (correlated color temperature). However, the general requirements also specify the ability to dim down to 20% of light output, and Cree's bulb is not dimmable. **—by Margery Conner**

▷**Cree**, www.cree.com.

Cree's proof-of-concept LED bulb delivers more than 1330 lumens and consumes 8.7W for an efficacy of 152 lumens/W.

Dell recommends Windows® 7 Professional.

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Philips wins $10 million L Prize for LED-based 60W replacement bulb

Philips Lighting North America has won the first award under the Department of Energy's L Prize competition. Philips submitted its entry in 2009, and the DOE has been field-testing the bulbs for the past 18 months. The bulbs had to meet or exceed these requirements: greater than 900 lumens at 10W or less for an efficacy of greater than 90W/lumen at a CCT (correlated color temperature) of 2700 to 3000K and a CRI (color-rendering index) of at least 90. The Philips bulb exceeded all of these requirements during the 18-month trial.

The announcement of the award made no mention of pricing; however, the original requirements called for a target retail price of $22 for the first year it was for sale, $15 for the second year, and $8 in the third year. Philips has said it plans to offer the bulb for retail sale as soon as early 2012. Philips will receive a $10 million cash prize as well as L Prize-partner promotions and incentives. To date, 31 utilities and energy-efficiency program partners stand ready to promote and develop markets for the winning product. Two other entrants in this category may be eligible for program-partner promotions, increasing the number of possible qualifying products to three.

The bulb uses a clever remote phosphor system to gain a spherical distribution of light, unlike earlier snow-cone-type LED bulbs. (For a teardown of a similar Philips bulb, see "Remote phosphors: Philips LED teardown, part 2," *EDN*, Feb 15, 2011, http://bit.ly/hCo8ft). **—by Margery Conner**

Philips' LED-based, 60W replacement bulb won the Department of Energy's L Prize.

▷**Philips Lighting North America**, www.usa.lighting.philips.com.

Atomic-scale films are critical to transistors

As IC manufacturers move past the problematic 28-nm node, films with thicknesses measured in angstroms are increasingly vital to the functioning of transistors and even to the ability to create patterns on the wafer. A science-fiction-like ability to deposit a uniform, pure layer of material only angstroms thick has become a gating skill in several areas of advanced IC manufacturing. The most obvious critical application for film deposition is the HKMG (high-k/metal-gate) stack with which foundries are struggling at 28 nm.

Randhir Thakur, executive vice president and general manager for silicon systems at Applied Materials, sketches the seriousness of the problem. "The industry is at a very early stage with HKMG," Thakur says. He does not expect mass production before 2014. In comparison, he expects to see the first 3-D transistors in 2013, reaching mass production in 2016.


On a finFET, the gate stack is the nearly invisible layer between the fin and the arched gate electrode that crosses over the fin (courtesy IMEC).

Steve Ghanayem, vice president and general manager for metal deposition and front-end processing at the company, further explains: "In HKMG processing, we are replacing one oxide film with four or five complete processes, including two layers of oxide, atomic-layer deposition of hafnium-oxide, annealing, and nitridization. The layers we are forming are as thin as 3 angstroms. By the 22-nm node, half the atoms in the gate stack are in the interfaces between these films. Very small changes in oxide growth or tiny numbers of trapped impurity atoms show up in model-level variations in mobility and threshold voltage for the transistors."

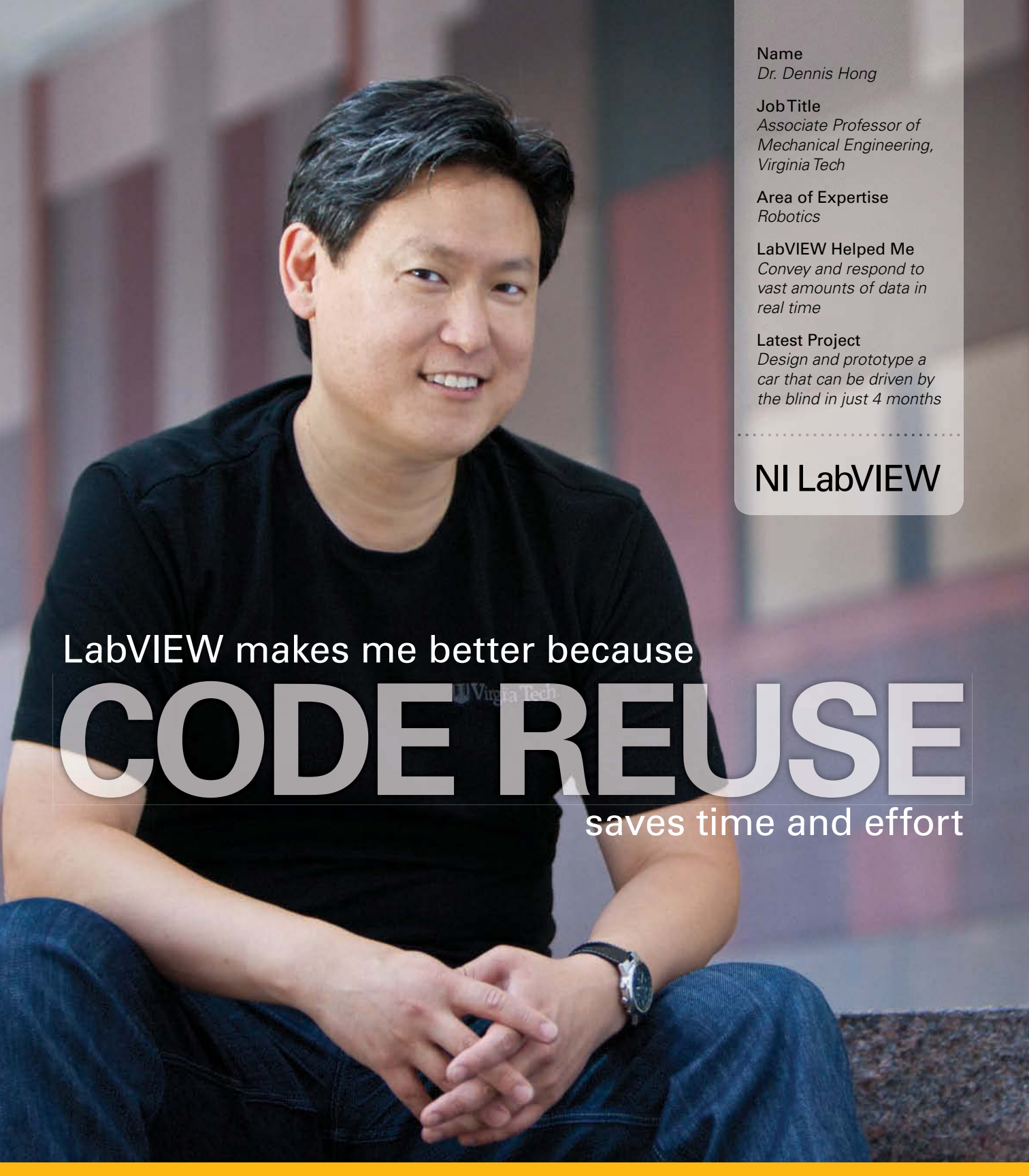
Once 3-D transistors, or finFETs, reach production, a new issue becomes critical: conformality. "We require 15 to 20 layers to form these 3-D-transistor structures," says Thakur. Worse than the sheer number of layers, though, is the shape. In planar processes, manufacturers deposit all of the films in the gate stack onto a flat surface or, at worst, onto the flat bottoms of shallow holes. For finFETs, however, the gate stack must lie across the fin like a saddle blanket, conforming to the right-angle corners at the edges of the fin and going straight down the sides. Any variation in the thickness of these films or any rounding or cracking at the corners shows up as variations in transistor parameters. Thus, processes must deposit atomic-layer films that conform almost perfectly to a surface comprising row upon row of tall, rectangular ridges.

Gate stacks are not the only issues. Girish Dixit, vice president for process applications at Novellus, points out that conformal film deposition is increasingly vital in lithography, as well. Each mask exposure now requires the deposition of several films: a hard mask, an antireflection layer that may itself include two or more films, and a resist layer. "Each of these films is usually conformal," Dixit says. In double- or quad-patterning scenarios, at least the hard mask must lie over a surface that has considerable topology, so the film must conform to complex ups and downs. In the case of a finFET process, the surface may have high-aspect-ratio features on it during the second phase of patterning. "Because the films are conformal, any roughness accumulates," Dixit adds. "And roughness will distort the pattern." Hence, these films must conform to the topology, and you must be able to smooth them to tolerances much finer than the feature size.

In many different steps, then, the ability to deposit unimaginably thin films, often over complex topology, has become necessary to creating transistors. Each variation in conformality, thickness, purity, or smoothness can appear to chip designers as a variation in transistor-model parameters. It is a game of angstroms. **—by Ron Wilson**

▷**Applied Materials**, www.appliedmaterials.com.

▷**Novellus**, www.novellus.com.



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VOICES

Silicon versus the bad guys: Infineon's Joerg Borchert on security

In advance of his ESC (Embedded Systems Conference) Boston keynote presentation, Joerg Borchert, vice president of chip-card and security ICs for Infineon Technologies North America, spoke to *EDN* about silicon-based security, privacy issues, market drivers, and user needs. An excerpt of that interview follows.

What are the key market drivers and user needs for silicon-based security?

A Silicon-based security is used in identification tokens for mobile phones, or SIM [subscriber-identification-module] cards; for payment cards to reduce fraud in debit- and credit-card schemes; in government IDs around the world; and in transport [ticketing and IDs]. When we are talking about embedded security, the market drivers are on one hand traditional, secure computing. An important vertical market is smart grid or, in a broader scheme, critical infrastructure. Then, it's safety meets security. We have to differentiate between safety and security. When a safety system fails, there is immediate and direct harm. A security system could harm or enable the ability to harm.

How does silicon-based security complement other security features while still protecting privacy?

A Security is mainly done today by software. There are some inherent issues with software, especially in the connected system. Silicon-based security can put an anchor into the system that allows the implementation of information assurance through an embedded system. Basically, that means management related to the use, storage, and transmission of information on a silicon level.

On the topic of privacy, recent attacks that have made people nervous targeted service providers, which hold large amounts of data. Better mechanisms to prevent these [attacks] are already [available] but may not be widely used. These [mechanisms] are for standard topics of information security, such as access-rights management combined with authentication, full disk encryption, trusted network-connection technologies, and combined use of trusted platform modules and service and protocols. If you combine that [group of mechanisms] with authentication methods, [you could prevent] a lot of these [attacks]. Security and privacy are topics that the industry has to become better at explaining, especially when it comes to these kinds of things in which the massive amount of user data is suddenly available and for sale.

What are the main vulnerabilities that chips are addressing in secure-identification documents?

A In the case of ePassports, the chip is in addition to existing security features. The threat scenario is different when you are talking about ID cards that can do electronics signatures. Then, you have to provide the highest security available. There have been documented attacks to smart-card ICs. We [at Infineon] believe that you have to constantly invest in security. It's a constant race with the bad guys. If you do electronics signatures, then you have to provide a best-of-class security level to prevent vulnerability.

What opportunities for silicon-based security do you see in NFC [near-field communications] and smart payments?

A We [estimate] that in the worldwide marketplace, [Infineon] will ship 50 million to 70 million NFC secure controllers this year. They can support [various] payment types; transport tools; and access [IDs], such as an access pass when you go into a company building. Last but not least, there are applications on the horizon, such as loyalty points, that can be on a phone. The NFC secure element is basically the hardware manifestation of an identity—a payment identity, your identity with a company, loyalty identity, or mass-transport identity—so you can hold your phone, swipe, and go.

What other opportunities do you see for silicon-based security?

A There's a tremendous opportunity in embedded systems in the future. Embedded systems are in everything from washing machines to mission-critical systems, which are programmable-logic controls in water and electricity supply. These embedded devices are connected and have a big impact. There's a good opportunity in the future. There will be more systems with embedded controllers that have to be secured than PCs [with Trusted Platform Module], for example, in the numbers of systems shipped this year.

You'll be speaking at ESC Boston in a few weeks. What key issues and trends will you address?

A I will address the key vulnerabilities, lessons learned from the PC and server-client architectures, applying things to the embedded side, what can be done better by taking into account life-cycle management, and applying information assurance and logic to those problems, as well as reliability. These issues are especially important to systems that have to perform, even if they are attacked.

—by Suzanne Deffree

For more information on ESC Boston, part of UBM's DesignDays event September 26 to 29, visit http://bit.ly/ESC_EDN.

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BY BONNIE BAKER

Get the job right the first time

It has been a long time since I checked into university-education programs for students who will be pouring into my profession. From my perspective, things look good. Senior projects have certainly improved since I went through my program. Recently, I had the pleasure of judging the Texas Instruments 2011 Engibous Prize Contest (named after TI's recently retired chairman, Thomas Engibous). TI holds intrauniversity contests in North America and invites the winning teams to compete for recognition and cash prizes.

Students, professors, sponsors, advisors, and the respective departments are the real heroes in this program. As a contest judge, I look for research, planning, design and simulation, building, prototype, and test stages in the analog, microcontroller, and processor content. During my review of 21 contest-finalist reports, I saw a variety of design projects and their implementations. The details in these designs outlined the circuit diagrams, layout, and firmware code. Many used multiple disciplines, such as organization, project feasibility, electronic, mechanical, firmware and software, and PC GUI (graphical-user-interface) programs.

The 2011 Engibous Prize Contest first-place winners are from Rice University (Houston). The design team, comprising Anthony Austin, Jeffrey Bridge, Robert Brockman II, and Peter Hokanson, chose Mars as their next frontier. To get the lay of the land before sending humans to Mars, the winning design team, Electric Owl, developed a flight-control electronics module for a fully autonomous unmanned aerial vehicle. The team's design considerations included Martian atmosphere, energy gathering, interplanetary transit, light-propagation delay for communications, and high-radiation environmental issues.

With this overwhelming project, the team decided to first develop flight-capable hardware with basic autopilot functions. Next, the team implemented redundant-sensor capabilities (**figures 1** and **2**). The fun began when they tested the prototypes. The team simulated six real flight tests during this project. On the first, they performed verification to ensure that the servo board correctly received, processed, and transmitted pulses with appropriate timing. During the second test, a three-board test using the backplane came to a premature end. Through this test, the team found a telemetry bug. It took two more flights to test the autopilot and two more to verify the redundant sensors.

Upon completing the design, the team designed and fabricated a set of avionics hardware for a fixed-wing, unmanned aerial vehicle. The hardware design was modular, separating the system's functions onto four types of PCBs (printed-circuit boards). The team wrote and tested the firmware, including a basic autopilot algorithm and a custom real-time kernel for the general-purpose computer board, for each PCB—not bad for a year of hard work!

Using analog chips, the team demonstrated the basic functions of the system operating with a triply redundant set of sensors in a real flight environment, installing the avionics package in a standard, off-the-shelf RC airframe. The plane successfully processed data from each set of sensors and used this data with the autopilot to get the plane to maintain a fixed heading. **Reference 1** provides a full project report and a video of the team explaining the project. The prize money is modest, but the experience for all the competitors in this contest was priceless. EDN

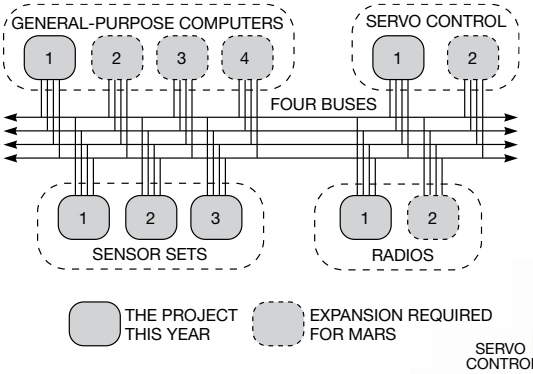


Figure 1 As part of the project, the winning design team, Electric Owl, implemented redundant-sensor capabilities.

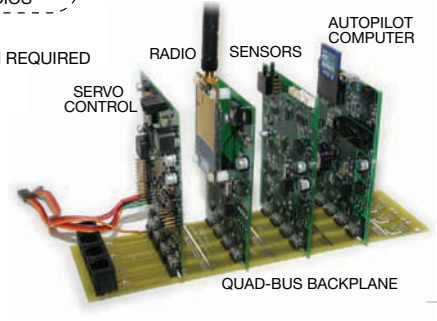
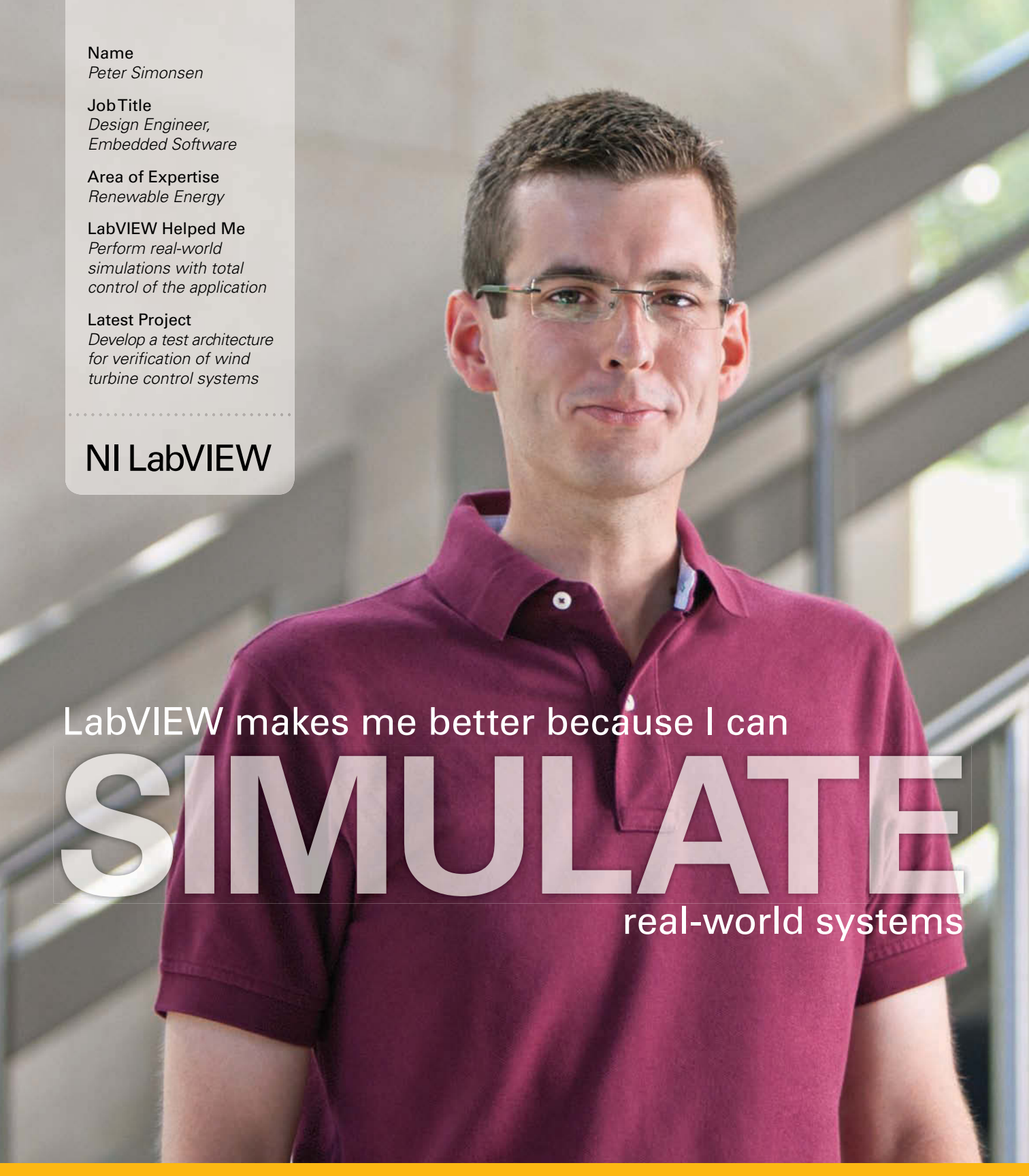


Figure 2 The team performed verification to ensure that the servo board correctly received, processed, and transmitted pulses with appropriate timing.

REFERENCE

1 The Engibous Prize, Texas Instruments, http://bit.ly/qhOeZZ.

Bonnie Baker is a senior applications engineer at Texas Instruments.



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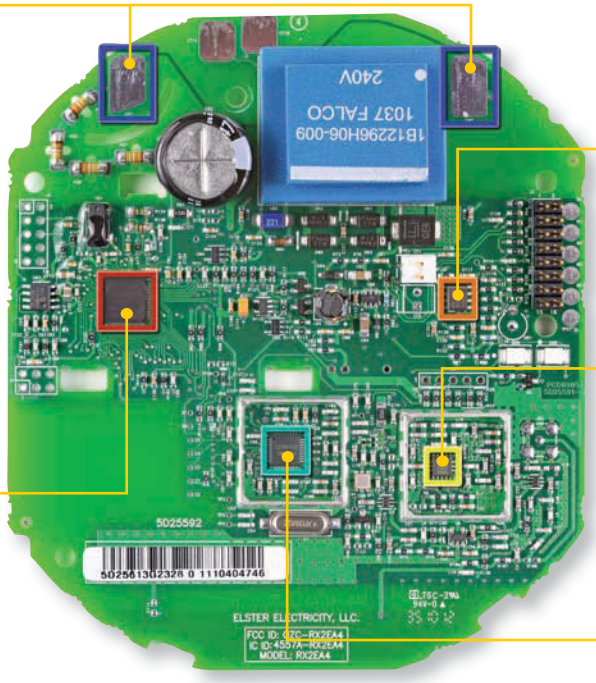
What's inside a smart meter? iFixit tears it down

You can usually find the folks at iFixit tearing down electronics with an eye toward expanding your knowledge of how to repair your electronic devices and keep them out of landfills (see "iFixit's Kyle Wiens: extending electronics' life span," *EDN*, Jan 21, 2010, http://bit.ly/nqwc0K). When iFixit's Chief Executive Officer Kyle Wiens had the opportunity to tear down an Elster (www.elster.com) smart meter, however, he jumped at it—not to produce a repair manual but to evaluate the health and safety issues that surround the utilities' installation of smart meters.

The technicians at iFixit got their hands on an Elster Rex2 Watthour meter with features that an old-fashioned motor-driven meter lacks: nonvolatile memory with 1 million write cycles, advanced security with full 128-bit AES (Advanced Encryption Standard) encryption, the ability to make remote upgrades, and support for 900-MHz and 2.4-GHz ZigBee communication. The meter can also track overall power usage by time, which raises privacy concerns for some utility customers. On the other hand, some customers welcome the ability to parse their power usage to better manage it and, they hope, save money.

The communication protocol is proprietary, although Elster supports ZigBee for in-house communication (www.energyaxis.com/ea-home.asp). For example, if a customer wanted to track and parse power usage in the home, Elster could turn on the ZigBee-network feature to communicate with a home-energy-management box. This feature is not standard in the Rex2 meter, however, and points out a possible business model for meter companies, given that the utilities have thus far not offered power-management features to residential customers.

The pads within the royal-blue boxes take 240V ac from the large copper wires into the blue transformer that steps it down to about 10V ac. The device rectifies, converts, and regulates the power to adjust to the smart meter's microcontroller and communications ICs.



The orange box encompasses a Texas Instruments low-power LM2904 dual operational amplifier.

The yellow box surrounds a medium-power RFMD RF2172 amplifier IC.

Inside the red box is a Teridian 71M6531F SOC with a microprocessor core, a real-time clock, flash memory, and an LCD driver (see "Teridian smart-power-meter-IC family offers alternative to current transformers," *EDN*, Feb 3, 2010, http://bit.ly/rdWw6A, and "Smart-power-meter-IC family offers alternative to current transformers," *EDN*, March 18, 2010, http://bit.ly/ocRjyr).

The pale-blue box outlines a less-than-1-GHz Texas Instruments CC1110F32 SOC with a microcontroller and 32 kbytes of flash memory.

To address health concerns about radiated energy when the smart meter communicates with the utility, Elster programs the meters for the time and frequency of transmission. For example, Pacific Gas & Electric, which uses smart meters from General Electric, says that its smart meters transmit for only approximately 45 seconds per day. According to iFixit, if a device were always on, there might be a cause for concern. If what PG&E states about the limited transmission time is true, however, your cell phones, Wi-Fi Internet, and microwaves would probably cause more damage to your body than a smart meter would.

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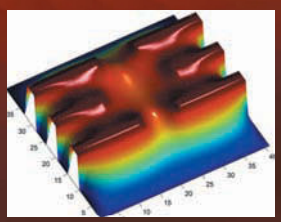

Modeling electric potential in a quantum dot. Contributed by Kim Young-Sang at HYU.

This example available at mathworks.com/ltc

Image: Kim Young-Sang, Jeong Hee-Jun, Quantum Device Lab, Hanyang Univ. ©2011 The MathWorks, Inc.

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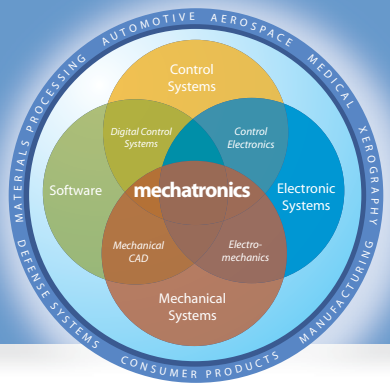

Control-oriented modeling for backlash

Backlash is complex; its model for control design is not.

By Kevin C Craig, PhD

In everyday language, the word "backlash" sounds as undesirable as its meaning: a strong adverse reaction or a violent backward movement. In engineering, the situation is no different. Backlash, the excessive play between machine parts, as often occurs in gears and flexible couplings, is undesirable and usually exists with compliance. It gives rise to inaccuracies in the position and velocity of a machine and to delays and oscillations.

For any physical system, a hierarchy of models is possible, from the most real, most complex, and more difficult to solve to the less real, less complex, and easier to solve. The model that is most beneficial for control design is the least complex model that still retains sufficient accuracy to capture the gross dynamic behavior of the system. It is critical to strike a delicate balance between dynamic complexity and accuracy in the model.

Figure 1 shows the physical system under investigation with the accompanying assumptions. In addition, assume that collisions due to backlash are sufficiently plastic to avoid bouncing. It is critical that the model capture the fact that the output from the backlash element causes a torque on—not a displacement of—the load inertia. This model also captures situations in which the assumed massless compliant element has damping (**Reference 1**). The following demonstration shows the importance of this model: Imagine that you are compressing with your hand a massless spring that possesses no internal damping. If you were to suddenly move your hand away, the spring would stay in contact because its response is instantaneous; being pure, it has no mass or damping. If the spring has damping and you repeat the experiment, however, the spring's response would not be instantaneous, and it would start to lose contact.

The model in **Figure 2**, developed from the system equations of motion, captures these essential attributes and fosters insight. You can easily implement it in MathWorks' Matlab or Simulink and effectively use it for control-system design. EDN

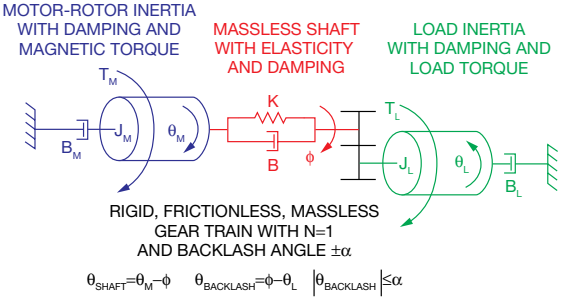

Figure 1 For the physical system under investigation, assume that collisions due to backlash are sufficiently plastic to avoid bouncing.

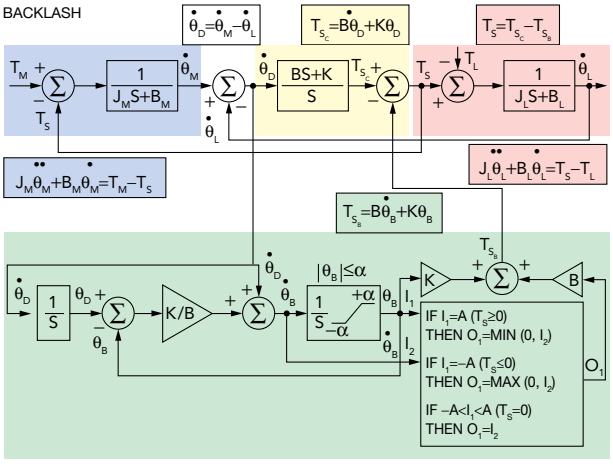

Figure 2 The model, developed from the system equations of motion, captures essential attributes and fosters insight.

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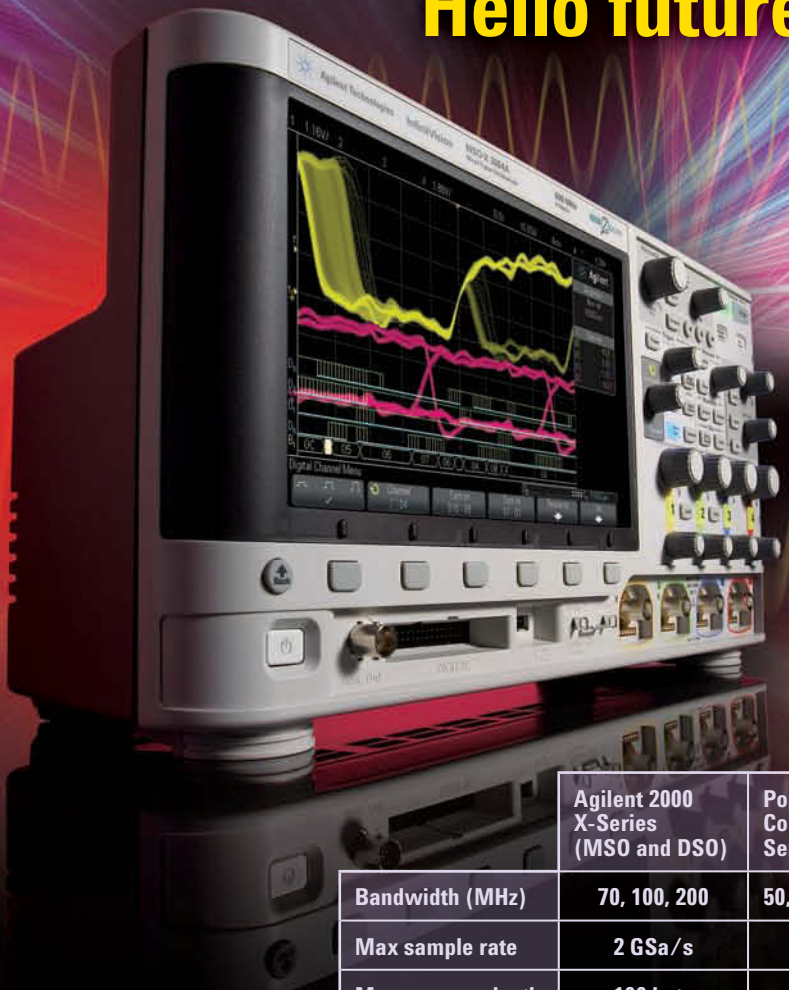
1 Nordin, Mattias, and Per-Olof Gutman, "Controlling mechanical systems with backlash—a survey," Elsevier Science Ltd, 2002, http://bit.ly/p8LfSb.

Hello future.



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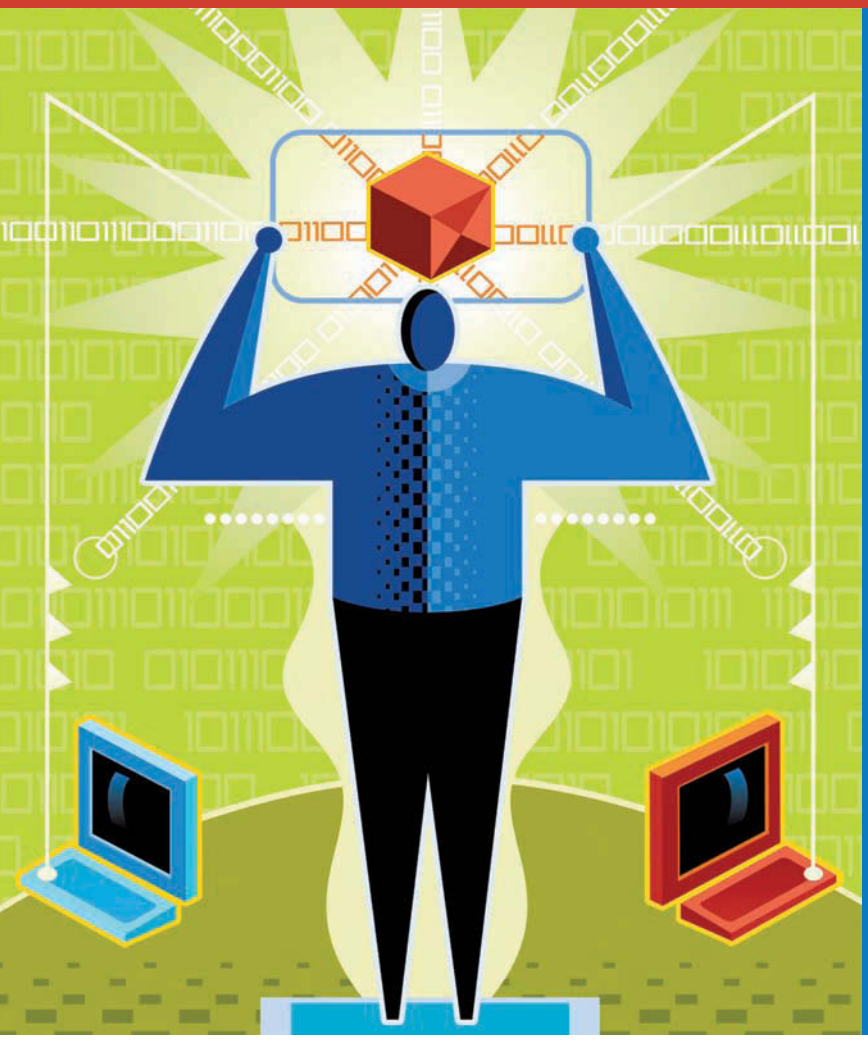

BY TIM KING • DDC-I

DEVELOPERS OF SAFETY-CRITICAL SOFTWARE CAN REAP THE BENEFITS OF MULTICORE PROCESSORS USING RTOS TECHNIQUES SUCH AS CACHE PARTITIONING AND SLACK SCHEDULING.

Designers optimize multicore processors for average-case execution time, often at the expense of worst-case, or longest, execution times. This trade-off presents significant challenges to developers of safety-critical software, who must design for worst-case behavior. Developers of safety-critical software can reap the performance benefits of multicore processors and still meet worst-case execution requirements by using modern RTOS (real-time-operating-system) techniques, such as cache partitioning and slack scheduling. Such techniques boost performance by enabling the system to more efficiently use memory and CPU without compromising safety.

IMAGE: GETTY

CPU throughput has roughly doubled every 18 months since 1985, consistent with Moore's Law. However, that trend began to slow around 2005 due to three key factors. First, memory speed has not kept up with CPU performance, increasing only about 10% per year during this time frame. Larger caches have helped alleviate the problem; even so, the memory subsystem remains a significant performance bottleneck.

The second factor is chip manufacturers' inability to deliver increased parallelism that applications can readily exploit. Theoretically, greater parallelism increases peak performance by enabling the CPU to concurrently process multiple instructions. Techniques such as pipelining, branch prediction, and speculative execution, however, have hit a wall, making it increasingly difficult to keep high-performance processors busy.

Thermal factors have also slowed the advance of CPU throughput. As operating frequencies increase, power consumption and heat generation also increase. Dissipating this heat presents difficult challenges in many environments, particularly for air-cooled, embedded systems.

Multicore processors have evolved to meet many of these challenges. To boost memory throughput, for example, each CPU core has its own L1 cache. Tighter physical packaging also boosts performance by shortening signal runs between cores, which makes data transfers faster and more reliable. Meanwhile, multiple cores enable processors to execute more instructions per clock cycle, permitting the cores to run at lower frequencies and thereby to consume less power and generate less heat.

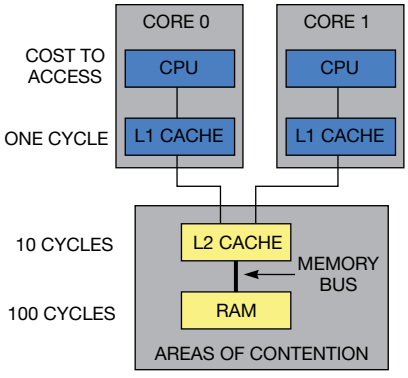

Figure 1 The latency to memory increases as you move up the hierarchy.

AT A GLANCE

- In mission-critical real-time systems, each task must have a worst-case time budget.
- Especially in multicore systems, the worst case may rarely occur, so a lot of time goes to waste.
- A slack-pooling algorithm can dynamically reallocate unused slack time to improve system performance.

MEMORY CONTENTION

Despite these advances, multicore processors still present key challenges for developers of safety-critical software. Chief among these challenges is increased contention for shared resources such as L2 cache and the memory subsystem. Consider a simple dual-core processor, each core with its own CPU and L1 cache and both cores sharing an L2 cache and a RAM subsystem (**Figure 1**). The example assumes an asymmetrical-multiprocessing system in which each core has a copy of the RTOS and a set of application software executing on it.

The values on the left side of the **figure** represent the cost that each CPU incurs when accessing a given resource. For example, say it costs one cycle for the CPU to access its local L1 cache. If that access misses and the CPU has to go to the L2 cache, it costs 10 cycles. If the L2 cache misses and the CPU has to go to RAM, the cost is 100 cycles. If the cache is "dirty" and requires write-backs, performance is even worse. Note that these numbers are inexact and vary from processor to processor, but the relative orders of magnitude are typical. The important point is that the farther out the CPU has to reach to access data, the more time the data transfer takes.

Contention arises when multithreaded processes on a CPU simultaneously compete for that core's L1 cache and when multiple cores simultaneously compete for the shared L2 cache or the memory subsystem. Even with a single-core processor, the CPU can easily overwhelm the memory subsystem. In a multicore system, multiple cores must contend for shared memory resources, so the memory-access bottleneck is worse.

CONTENTION AND SLACK

In safety-critical systems, a thread, sometimes known as a task or a process, must have a time budget that is adequate for its worst-case execution time. Even if the L2 cache is dirty from the thread's perspective and there is contention for memory, the thread must have budgeted sufficient time to complete its intended function. Otherwise, unsafe conditions, including the loss of equipment or human life, may arise.

Because worst-case execution scenarios rarely occur, threads typically experience something close to their average-case execution time. Occasionally, a thread exceeds its average-case execution time. However, if the thread's budget is set for its worst-case execution time, the typical result will be a lot of budgeted but unused time. Consider, for example, a thread that has a 500-µsec time budget. If the thread's average-case execution time is 300 µsec, that budget leaves 200 µsec of slack—budgeted but unused time per execution period.

Even on a single-core processor, a thread's worst-case execution time is typically much higher than its average-case execution time due to resource contention. For example, if Thread A pushes Thread B from the L2 cache, then Thread B must access the memory subsystem, which is often an order of magnitude slower. Again, worst-case execution times are even worse in multicore systems due to increased contention among the cores.

RESOURCE CONTENTION

Developers of safety-critical software face three key multicore-driven challenges: how to minimize resource contention, how to determine a thread's worst-case execution time so that the developer can set a safe time budget without overallocating time and generating copious amounts of slack, and how to put slack time to good use. At the interface between the L2 cache and the memory subsystem, there is contention for the memory bus and contention when accessing a bank of RAM. One way to reduce contention for physical RAM is to partition it. Some multicore processors, for example, lend themselves to board designs in which each

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core effectively has its own dedicated RAM and memory bus. This organization effectively creates a hardware partitioning, thereby eliminating contention at this level.

Memory-bus contention is difficult to address because processor manufacturers typically provide no documentation for bus-arbitration algorithms, such as bus priorities, scheduling and queuing, and burst sizes. The vendors also provide no means for software to control the bus. Nevertheless, processor manufacturers are beginning to recognize the importance of access to memory-bus internals, and they are making progress in this area.

There is also potential for contention at the interface between each core's CPU and the L1/L2 caches. Multiple threads within a core compete for the core's L1 cache. Threads on different cores, meanwhile, compete for their shared L2 cache. Traditionally, designers have used three caching policies to reduce contention and minimize the delta between a thread's worst-case execution time and its average-case execution time. The most rudimentary policy involves disabling the cache, which greatly reduces the difference between a thread's worst- and average-case execution times. Unfortunately, this policy essentially cripples the CPU because every cache access becomes a miss and requires an external-RAM access.

An alternative to disabling the cache is to lock critical code or data into given cache lines. This policy ensures high cache-hit rates for a relatively small amount of application code, but the rest of the software must compete—with increased contention—for the remaining nonlocked cache. Cache locking essentially picks winners and losers, and most are losers.

Another alternative to disabling the cache is to use a partition—flushing the cache before it enters a new process. In this way, each process starts with a clean slate and can fill the cache early in its execution and benefit from high cache-hit rates thereafter. The problem with cache flushing is that processor manufacturers optimize caches for desktop/server applications. In these systems, the minimum time is usually 10 msec, so once an application gets control of the CPU, it runs for at least 10 msec and usually much longer before something pre-empts it. This interruption gives the software time to prime the cache and achieve a cache-hit rate of more than 99% thereafter.

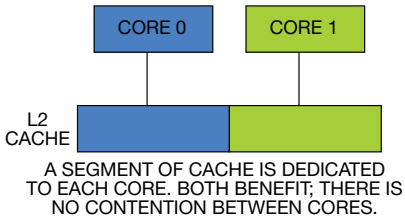

Figure 2 By physically partitioning the L2 cache, designers eliminate contention at that level.

In real-time safety-critical systems, by contrast, dozens or hundreds of threads typically execute within a typical 10-msec window. As a result, these threads don't have the time to prime the cache in their favor, so they experience much lower cache-hit rates and pound harder on the memory subsystem. Cache flushing is an improvement over disabling the cache but is still ineffective for most real-time safety-critical applications.

A better policy is to partition the cache, thereby dedicating a segment of the cache to each core (**Figure 2**). This physical partitioning reduces the total amount of cache available to each core. Overall contention decreases, however, because multiple cores no longer share the same resource. The DDC-I (www.ddci.com) Deos safety-critical RTOS, for example, uses this cache-partitioning policy.

SLACK SCHEDULING

As previously noted, resource contention forces developers to set safety-critical thread budgets for worst-case execution time, which can be significantly higher than average-case execution time. Further, multicore processors exacerbate that problem. The net result is that safety-critical software systems often have a significant amount of slack.

A number of commercial tools are available to help developers calculate and test each thread's worst-case path. To force worst-case cache effects, designers should also use a cache "trasher." Before running the thread under test, the cache trasher ensures that the cache is dirty. Further, if something pre-empts the thread under test during the test, the cache trasher again ensures that the cache is completely dirty from the thread under test's perspective. In this way, the thread under test gets the least benefit from the cache, thereby yielding a solid worst-case execution time for that thread.

Once designers have determined and budgeted for each thread's worst-case execution time, the challenge becomes how to put all of the generated slack to good use. In most real-time operating systems, the slack simply goes to waste or, at best, performs rudimentary background processing. A more efficient approach is to harvest the unused slack on the fly and make it available to other threads.

CACHE LOCKING LOCKS CRITICAL CODE OR DATA INTO GIVEN CACHE LINES. IT ESSENTIALLY PICKS WINNERS AND LOSERS, AND MOST ARE LOSERS.

At the beginning of any given period, a set of threads—T1 to TN, for example—are ready to run or will become ready to run. A certain amount of unbudgeted time, or head room, is also available. Harvesting puts this unbudgeted time—100 msec, for example—into a "slack pool." Think of the slack pool as an account for banking slack time. A harvesting algorithm

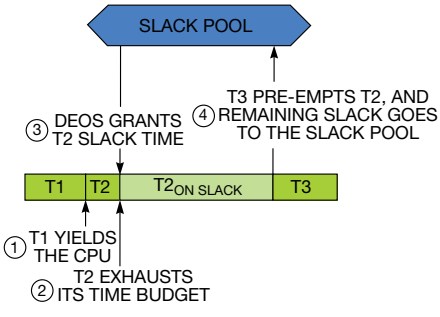

Figure 3 A slack pool allows tasks to run beyond their scheduled completion time.

then starts scheduling threads and giving them control of the CPU.

Consider an example (**Figure 3**). Suppose that the operating system gives control to T1 first and that T1's worst-case-execution-time budget is 600 µsec. Also assume that T1 executes and hits its average-case execution time, say 400 µsec. The operating system adds the remaining 200 µsec to the slack pool, thereby increasing the total slack in the pool to 100.2 msec.

Next, say that the OS schedules T2 and that T2's worst-case-execution-time budget is 200 µsec. Further assume that the programmer has declared T2 as "slack-enabled." Assume that once T2 begins to run, it uses its entire 200-µsec time budget. If T2 does not yield the CPU and if nothing pre-empts it, the OS will intervene, noting that T2 is slack-enabled, and add the 100.2-msec time in the slack pool to T2's time budget. T2 can then continue executing on slack time until it exhausts its slack-adjusted budget; until it yields the CPU, in which case any remaining budget goes to the slack pool; or until a higher-priority thread, such as T3, pre-empts it, in which case any remaining budget also goes back to the slack pool.

USING SLACK

Slack time may be unavailable when a slack-enabled thread could use it. Further, the operating system may not make fairness guarantees regarding allocation of slack. Nevertheless, you can effectively use slack in certified safety-critical systems in a number of ways. Some threads, for example, are simply noncritical: In Radio Technical Commission for Aeronautics' (www.rtca.org) DO-178B terminology, they'd have a design-assurance level of E (**Reference 1**). These threads, including such tasks as built-in test, are pure slack consumers. They have no allocated time budget and run purely on slack.

Other threads fall into the quality-of-service category. They must meet a minimum performance level, but, if time is available, they can provide a better result. A moving-map display is a good example. On one aircraft, system safety analysis and human factors show that this display requires 10-Hz update rates to avoid jerky movement that could induce eye fatigue in pilots. Even at 10-Hz, however, the update isn't particularly smooth. The solution is to give the moving map's thread enough time to ensure a 10-Hz update rate and to designate it as slack-enabled. By using slack, the thread almost always achieved a 20-Hz or better update rate. Consequently, the moving map is smooth, and pilots love it.

Slack also works well for "anytime algorithms," which produce good answers in a given amount of time but produce better answers in a greater amount of time. For example, the more time you give an interpolation algorithm to iterate, the more precise the answer it yields will be. Again, allocate enough time to generate a good-enough answer and use slack when available to generate a better answer.

Slack scheduling is not simply background processing, though you can use it in that manner. The key distinction is the ability to dispense slack time throughout a period rather than to save it up for use at the end of a period. This distinction enables more interesting and useful features. The ability to recover and use slack is essential for real-time safety-critical systems, in which the need to budget for worst-case versus average-case execution times makes it difficult to use available CPU cycles. Slack scheduling is particularly important for multicore systems, in which contention for cache and other memory resources greatly increases worst-case execution time. Techniques such as cache partitioning can help alleviate this contention, but the ability to reuse slack is crucial for unleashing the full potential of multicore processors in safety-critical applications. EDN

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AUTHOR'S BIOGRAPHY

Tim King is the technical-marketing manager at DDC-I. He has more than 20 years of experience developing, certifying, and marketing commercial avionics and real-time-operating-system software. King received a master's degree in computer science from the University of Iowa (Iowa City, IA) and a master's degree in business administration from Arizona State University (Tempe, AZ).

GaN and SiC:

ON TRACK FOR SPEED AND EFFICIENCY

WIDE-BANDGAP MATERIALS, **SUCH AS GaN AND SiC,** ARE ENABLING A NEW GENERATION OF POWER SWITCHING DEVICES THAT SWITCH FASTER AND WITH FEWER LOSSES THAN THE VENERABLE SILICON MOSFET, RESULTING IN SMALLER, MORE EFFICIENT POWER SUPPLIES.

BY MARGERY CONNER • TECHNICAL EDITOR

Silicon power MOSFETs are approaching their theoretical performance limits for both on-resistance and gate charge. Although silicon switches will continue to eke out gains, the increases will come more slowly and be smaller. Enter wide-bandgap materials: SiC (silicon carbide) and GaN (gallium nitride). Both technologies have for several years found use in RF amplifiers. Advances in process manufacturing are driving down the costs and increasing the power capability of power switches employing these materials, and proponents of both claim that they will supplant silicon MOSFETs in switched-mode-power-supply designs in which power density and efficiency are key attributes.

IMAGE COMPOSITE: DAVID NICASTRO; IMAGES: ISTOCKPHOTO

The size of a power supply's components determines its power density; the largest components are the inductors and capacitors, and the MOSFET is a distant third. Capacitors and inductors shrink with higher switching frequency, which is topping out for silicon MOSFETs. Switching losses due to the gate charge would cancel any further increase in switching speed. As for the MOSFET itself, shrinking the die of a silicon MOSFET unfortunately increases the on-resistance. MOSFETs have traditionally measured their performance figure of merit as the on-resistance times the gate charge. For silicon devices, one parameter trades off against the other. Decreasing on-resistance usually comes from increasing the area of the device, but that increase in area comes with an increase in gate charge and, hence, capacitance, which decreases the device's speed.

Wide-bandgap materials have lower on-resistance by an order of magnitude than silicon materials, with no correspondingly great increase in gate charge. The problems have been the difficulty and expense of working at high power with GaN and SiC materials. GaN and SiC transistors have for years found use in RF amplifiers, and SiC Schottky diodes commonly work as rectifiers in high-voltage power supplies because they have a fraction of the reverse-leakage current of silicon diodes. In addition, SiC has a high thermal conductivity, so an increase in temperature doesn't degrade the device's switching parameters. SiC devices target high-voltage applications that require a blocking voltage of 1200 to 1700V. At these voltages, silicon IGBTs (insulated-gate bipolar transistors) are more common switching devices than MOSFETs, but IGBTs are more expensive, and fewer engineers are familiar with IGBTs' design constraints. SiC FETs share some of the same drive characteristics as silicon MOSFETs, such as being normally off, and can take advantage of MOSFETs' relatively large base of design engineers.

AT A GLANCE

- Silicon MOSFETs are approaching their theoretical limits for both on-resistance and gate charge.
- Both SiC (silicon-carbide) and GaN (gallium-nitride) power transistors have significantly higher figures of merit, especially at high blocking voltages, than those of silicon MOSFETs.
- SiC FETs shine at 1000V and higher, whereas GaN devices are currently at 200V and below. Several companies plan to announce 600V and higher-voltage GaN devices at the end of 2011, however.

THE NEARLY $100 PRICE OF SiC MOSFETs MAY CONDEMN THEM TO NICHE MARKETS, BUT IT'S ALSO LIKELY THAT THEY SELL AT THAT PRICE BECAUSE THAT'S WHAT THE MARKET WILL BEAR.

Figure 1 Cree's CMF2012SD series FETs compete with 900V silicon-based MOSFETs and 1200V IGBTs.

Among available SiC power MOSFETs is Cree's recently introduced SiC CMF2012SD series. The $93.75 devices have a 1200V blocking voltage and a maximum on-resistance of 110 mΩ at a drain current of 20A and a gate-to-source voltage of 20V (**Figure 1**). On-resistance increases by only 20% at the maximum operating temperature of 150°C. The devices have a gate charge of less than 100 nC throughout the input-voltage range, simplifying gate-drive requirements, and the devices have a forward-voltage drop of less than 2V at a 20A load current, reducing losses. Cree also offers the Z-Rec rectifier, a companion family of SiC power diodes, which has essentially no reverse recovery at 600, 650, and 1200V breakdown voltages. The devices have current ratings of 1 to 20A at 600V, 4 to 10A at 650V, and 5 to 20A at 1200V. The devices are also available in chip form with currents of 10 and 25A at 1700V.

Also in the market, Rohm Semiconductor recently announced its SCS1xxAGC series of SiC Schottky diodes, which maintains low forward voltage over a wide operating-temperature range. For example, the 10A-rated SCS110AGC part has forward voltage of 1.5V at 25°C and 1.6V at 125°C. The short typical reverse-recovery time of 15 nsec enables high-speed switching and minimizes switching loss. Prices range from $6.38 for the 6A version to $24.60 for the 20A version. Rohm will this year follow up its SiC diodes with SiC FETs; it also plans to release 600V transistors in Japan with 1200V SiC FETs in 2012. SemiSouth also makes SiC Schottky-diode rectifiers for solar-inverter and power-factor-correction applications and offers a SiC power JFET, the normally on 1200V SJEP120R085.

The nearly $100 price of SiC MOSFETs may condemn them to niche markets, but keep in mind that, when silicon MOSFETs debuted more than 30 years ago, their prices were also around $100 (in 1970s dollars), yet they now sell for a few dollars each. John Palmour, chief technology officer at Cree, expects the same downward trend in price for SiC devices, in large part because of the room for manufacturability and manufacturing efficiency (**Reference 1**). However, it's also likely that SiC devices sell at their current price because that's what the market will bear. Power efficiency has a price, and more efficient power supplies pay off in energy savings.

GaN devices have also had initial success as RF switching devices, generally at lower voltages than those of SiC. Manufacturers grow the GaN devices on sapphire substrates, involving high manufacturing costs. The breakthrough for GaN came with the ability to grow

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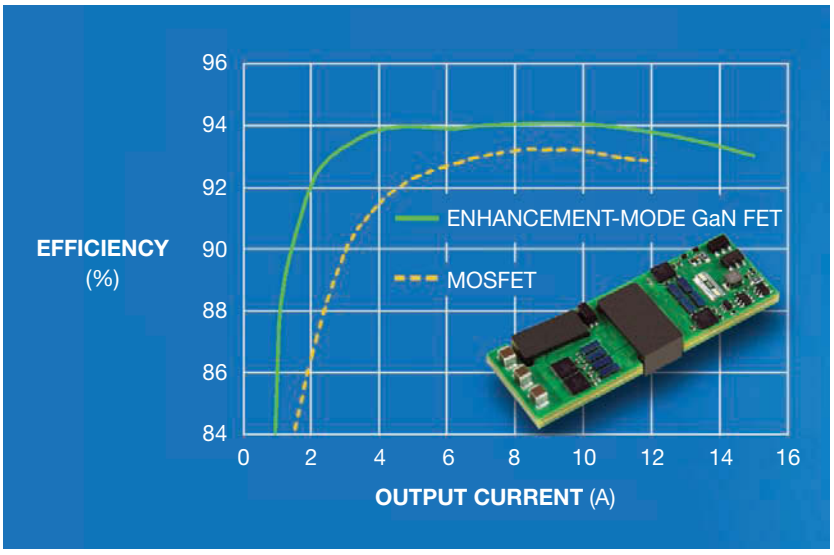

Figure 2 National Semiconductor's LM5113 high- and low-side GaN-FET driver regulates the high-side floating bootstrap-capacitor voltage at approximately 5.25V to drive EPC's eGaN power FETs without exceeding the maximum gate-to-source voltage rating.

GaN structures on silicon. Initial GaN-on-silicon devices all operated at less than 100V, targeting use in the datacom-power-conversion market. GaN's higher switching speed and efficiency allow dc/dc converters to operate in the megahertz region, saving space, reducing the need for heat sinks, and conserving power. International Rectifier was the first company to offer GaN-on-silicon power switching devices to the commercial market with the introduction of the IP2010 in late 2010. The device has a blocking voltage of 20 to 40V and targets point-of-load dc/dc converters. The company's technology operates in depletion, normally on, mode but hides this characteristic from designers because the company offers the parts as complete driver stages rather than as discrete devices. For example, rather than quote a blocking voltage for the FETs, International Rectifier quotes the GaNpowIR stage by its input-voltage range of 7 to 13.2V, output voltage of 0.6 to 5.5V, output current of 30A, and operating frequency as high as 3 MHz. The drivers sell for $9 (2500).

EPC (Efficient Power Conversion) also offers GaN devices, for which it uses the trademarked name eGaN (enhanced-mode GaN). The company recently introduced the EPC2010 FET, which has a drain-to-source voltage of 200V, a maximum on-resistance of 25 mΩ with 5V applied to the gate, and a pulsed-current rating of 60A. Unlike International Rectifier's GaN power-conversion-stage device, the EPC2010 is a discrete transistor. The drive is similar to a silicon power MOSFET, but some challenges in driving one exist. For example, because of the high switching frequencies, an eGaN circuit is sensitive to layout. The device also tolerates only a narrow range of gate voltages. To ensure that it's on requires 4.5V, but it can tolerate only 6V. Considering the power transients you can expect in a power-converter environment, 1.5V is a narrow range of operation. Because the threshold is lower, you must drive it even harder when the gate gets close to ground to ensure that it stays below 1.4V rather than the 2.5V threshold you would encounter in a silicon MOSFET.

"There's no true body diode in a GaN FET," says Alex Lidow, founder and chief executive officer of the company. "There's no reverse recovery loss, which is a performance gain. But when you do leave the FET on, it still has a forward drop of greater than 1.5V, so you have to be careful about dead time. None of these [drawbacks] are insurmountable, but you have to be careful."

Recognizing an opportunity, National Semiconductor recently introduced a 100V half-bridge gate driver for use with eGaN FETs in high-voltage power converters (**Figure 2**). The LM5113 high- and low-side GaN-FET driver regulates the high-side floating bootstrap-capacitor voltage at approximately 5.25V to drive eGaN power FETs without exceeding the maximum gate-to-source voltage rating. The LM5113 also features independent sink and source outputs for flexible turn-on strength with respect to the turn-off strength. A 0.5Ω-impedance pulldown path provides a fast, reliable turn-off mechanism for the low-threshold-voltage eGaN power FETs. The LM5113 also integrates a high-side bootstrap diode, further minimizing PCB (printed-circuit-board) real estate, and provides independent logic inputs for the high- and the low-side drivers, enabling flexibility for use in a variety of both isolated- and nonisolated-power-supply topologies.

As for the future of GaN power devices, International Rectifier and EPC have both preannounced prod-

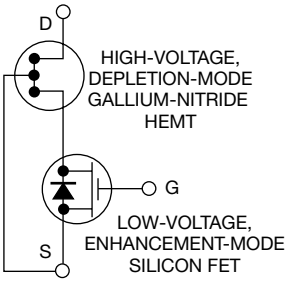

Figure 3 International Rectifier pairs a low-voltage silicon-FET gate driver with a high-voltage GaN HEMT in a cascode configuration, resulting in an enhanced-mode switch with the drive characteristics of a silicon MOSFET.

FOR MORE INFORMATION

Cree
www.cree.com

Efficient Power Conversion
www.epc-co.com

International Rectifier
www.irf.com

MicroGaN
www.microgan.com

Microsemi
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ucts for release by year-end with drain-to-source blocking voltages of 600V. International Rectifier's new device (**Figure 3**) will depart from its original GaN-based power-converter stage and be a discrete switching device that pairs a low-voltage silicon FET in a cascode configuration in series with a GaN HEMT (high-electron-mobility transistor), meaning that "you get normally off operation in a three-terminal device whose drive looks and acts exactly like a typical silicon-based power [device]," says Tim McDonald, vice president of emerging technologies at the company. Further, you can drive it with standard gate drivers, with no special considerations about voltage limitations, overvoltage, or reliability, he adds.

GaN-power-device vendor Transphorm made its first public announcements at this year's Applied Power Electronics Conference. It plans to introduce fully qualified 600V devices with on-resistances as low as 180 mΩ by the end of the year. The company uses both silicon and SiC substrates for its GaN devices, building early versions of its parts on SiC, which has a crystal structure that's closer to GaN, and troubleshooting the process on SiC before it moves it to silicon. The device structure will be similar to International Rectifier's approach, cascoding a low-voltage silicon FET in series with a high-voltage GaN HEMT (**Reference 2**).

"We looked at the problem of creating a normally off device in GaN and decided that the state of the art for GaN-gate construction limited the maximum positive voltage to 6V," says Carl Blake, Transphorm's vice president of marketing. "We viewed this [limitation] as a serious problem, which would limit the practical use of high-voltage GaN devices, so [we] decided to package two dice in a single package using the proven silicon technology as the current controller and the new GaN as an improved voltage-blocking device." This approach enables power-design engineers to use available controllers and drivers and to focus on rapid performance improvement, he explains.

EPC has also preannounced 600V eGaN devices. According to EPC's Lidow, no fundamental limitation exists for GaN devices' blocking voltage, and GaN will rival and cost less than SiC for high-speed devices. It has come as a surprise to him that new applications have started using GaN simply as a silicon-MOSFET replacement. One such application is RF envelope tracking, he says. Lidow likens this application to a dc/dc power supply except that it follows the modulated signal up and down, creating an envelope that always biases the transistor a couple of volts higher than what it needs to generate an amplitude signal. This technique eliminates the heat that goes to waste in the transmitter. He says that the use of GaN enables power supplies to change their voltages when operating at 100 MHz, adding, "The most expensive part of an RF system is the transmitter, and now it has unloaded all of the waste energy that's heating it up, allowing you to either pump out twice the power or eliminate some heat sinks."

Lidow sees solar microinverters as other likely applications. The approximately 250W inverters find use in homes or businesses and compete in efficiency with 3-kW central inverters, which are currently more efficient than the lower-power, lower-voltage microinverters. The microinverters' simultaneous requirements of high frequency, high voltage, and high power make the use of GaN HEMTs attractive.

Many industry participants believe that the second-source market for these new parts will mimic the early stages of the silicon MOSFET market and that many companies will jump in with their own takes on the technologies. For example, Microsemi plans to partner with EPC to develop a high-reliability version of EPC's GaN HEMT. EDN

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When absolute accuracy and repeatability are critical over temperature ranges of –200 to +800°C, PRTDs are the best choices for precision industrial and medical applications. Platinum is stable, and corrosion and oxidation do not affect it. Nickel, copper, and other metals also can be used for RTDs, but those materials are less popular because they are less stable and repeatable than platinum.

Modern PRTD standards, such as the IEC (International Electrotechnical Commission) 60751 and the ASTM (American Society of Testing and Materials) 1137, allow substantial interchangeability of sensors among systems based on their specified tolerance and temperature coefficients. These standards make it easy to replace a sensor with one from the same or a different manufacturer and ensure rated performance with minimal redesign or recalibration of the system.

Three common PRTDs are the PT100, PT500, and PT1000, which exhibit resistance values of 100, 500, and 1000Ω, respectively, at 0°C. Higher-resistance devices, such as the PT10000, are available at a slightly higher cost. PT100s were more popular historically, but today the trend is toward higher-resistance values that provide higher sensitivity and resolution at little or no extra cost. Typical of these is the PT1000, whose 0°C resistance is 1 kΩ.

Manufacturers such as Vishay Intertechnology (www.vishay.com) and Jumo (www.jumo.net) now offer PRTDs in the standard SMD (surface-mount-device) sizes, with typical prices in the low-single-digit-dollar range, depending on the value, size, and tolerance. Such devices substantially reduce sensor cost and provide designers with the flexibility to place PRTDs on any type of PCB (printed-circuit board). The following example includes Vishay Beyschlag's (www.vishay.com) popular and cost-effective, 1000Ω PTS1206 (**Reference 1**).

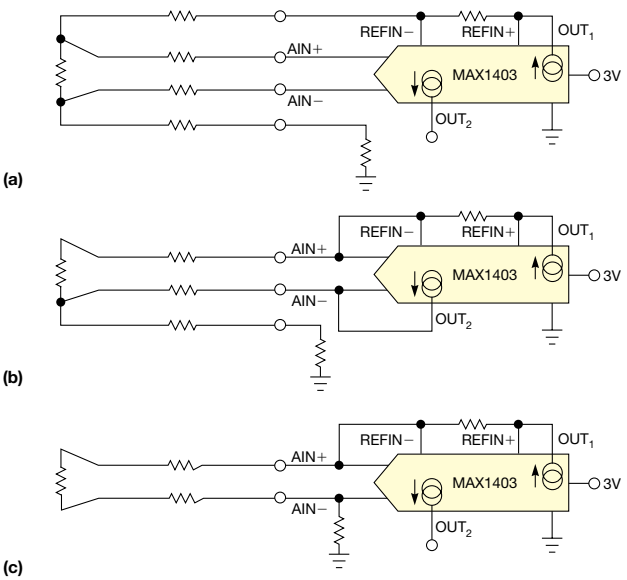

Figure 1 A PRTD can sense temperature using an interface of four wires (a), three wires (b), or two wires (c), each delivering a differential signal to the ADC.

A traditional method for PRTD measurement is current-source excitation (**Figure 1**). For measurements at a distance and with dissimilar lead wires, the four-wire Kelvin-connection approach of **Figure 1a** gives the most accurate results by separating the current-carrying wires from the measurement wires. OUT_1 provides a 200-µA source for the PRTD, and OUT_2 remains floating in this configuration. Most industrial applications in which the RTD element is not close to the ADC require fewer wires because each wire adds to the system cost and reliability concerns.

The three-wire temperature-sensing technique of **Figure 1b** is more economical and provides accurate readings if the lead wires are similar, so it is the most popular. The two

TABLE 1 MAX11200 KEY SPECIFICATIONS

Parameter	MAX11200	Comments
Sample rate (samples/sec)	10 to 120	Variable oversampling rate can be optimized for low noise and for –150-dB line-noise rejection at 50 or 60 Hz
Channels	One	GPIOs allow external multiplexer control for multichannel measurements
Maximum integral nonlinearity (ppm)	±10	Provides good measurement linearity
Offset error (µV)	±1	Provides almost zero offset measurements
Noise-free resolution (bits at samples/sec)	19 at 120, 19.5 at 60, 21 at 10	High dynamic range with low power
V_{DD} (V)	Analog V_{DD} (2.7 to 3.6) Digital V_{DD} (1.7 to 3.6)	Analog and digital V_{DD} ranges cover the industry's popular power-supply ranges
Maximum I_{CC} (µA)	300	High resolution per unit power for portable-system applications
GPIOs	Yes	Allows external device control, including local multiplexer control
Input range	0 to V_{REF}, ±V_{REF}	Input ranges are wide
Package	16-pin QSOP, 10-pin 15-mm² µMAX	10-pin µMAX works in space-constrained designs

matched current sources of the ADC cancel the IR errors due to lead-wire resistance. OUT_1 and OUT_2 both source a 200-µA current.

The two-wire technique of **Figure 1c** is the most economical, and is used only when the parasitic wire resistance is known and unchanging. You compensate for IR errors of the wires by computation within a microcontroller or a DSP. The higher resistance in a PT1000 PRTD makes it less sensitive to lead-wire resistance and lowers its self-heating error, so you can connect it directly to the ADC, even in a two-wire configuration. A delta-sigma ADC is suitable for sampling various types of PRTDs. **Table 1** lists some important characteristics of this ADC.

As an alternative to current excitation, you can excite the PRTD with a precision voltage source. Voltage excitation is more desirable for higher-resistance PRTDs, and the same voltage reference that biases the ADC can be used to bias the PRTD. You can connect a PRTD directly to the ADC, with the ADC's reference providing PRTD bias current through one precision resistor (**Figure 2**). The ADC then accurately and ratiometrically measures temperature.

If the lead-wire resistances are orders of magnitude lower than the current-limiting resistor, R_A, and the PRTD resistance at t°C, R_T, you can calculate the voltage across the sensor, as the following **equation** shows:

$$V_{RTD}=V_{REF}\times\left(\frac{R_T}{R_A+R_T}\right),$$

where V_{REF} is the ADC's reference voltage. The following **equation** provides another expression for the sensor voltage:

$$V_{RTD}=V_{REF}\times\left(\frac{A_{ADC}}{FS}\right),$$

where A_{ADC} is the ADC output code and FS is the ADC full-scale code—that is, 2^{23}–1 for the IC in a single-ended configuration. Combining the two **equations** lets you solve for R_T:

$$R_T=R_A\times\left(\frac{A_{ADC}}{FS-A_{ADC}}\right).$$

This **equation** makes clear that R_A must meet certain precision requirements that the R_T specification dictates.

PRTD SELECTION AND ERROR ANALYSIS

Lead-wire resistance can introduce errors. Because the PRTD is a resistive sensor, connecting copper extension wires between it and the control instrument introduces resistance

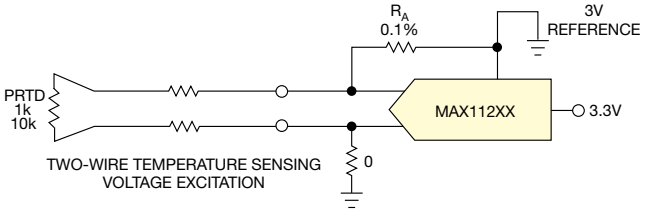

Figure 2 The sensing technique in this circuit employs voltage excitation, which works best with higher-value PRTDs.

TABLE 2 WIRE-GAUGE RESISTANCE VALUES

Copper lead wire (AWG)	Resistance at 25°C (Ω/foot)
16	0.0041
18	0.0065
20	0.0103
22	0.0161
24	0.0257
26	0.0418
28	0.0649

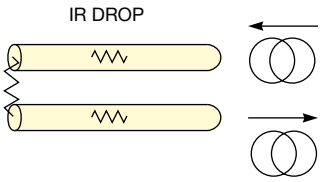

Figure 3 IR drops in the wires of a two-wire-sensing technique can produce errors at the ADC.

and adds error (**Figure 3**). To estimate the errors in a two-wire circuit, multiply the total length of the extension leads by the resistance per foot for AWG copper wire (**Table 2**). For example, assume that you want to connect two 3-foot lengths of AWG #22 wire to a PRTD. You can solve for the lead-wire resistance using the following **equation**:

$$R_W=2\times(3\ FEET)\times(0.0161\Omega/FEET)=0.1\Omega,$$

where R_W is the wire's resistance. For a PT100 in a 1206 package with 100Ω nominal resistance, the average sensitivity is 0.385Ω/°C. You can now calculate the wire error:

$$T_{WER}=R_W/0.385=0.26°C,$$

where T_{WER} is the error in temperature reading due to the lead wires, which equals R_W/S, and S is the average PRTD sensitivity. For a PT1000 in a 1206 package with 1000Ω nominal resistance, the average sensitivity is 3.85Ω/°C. You can now calculate the wire error:

$$T_{WER}=R_W/3.85=0.026°C.$$

According to the IEC 60751 standard, a T_{WER} of 0.026°C for the PT1000 is one order of magnitude less than the Class F0.3 tolerance of ±0.3°C, meaning that you can use a 3-foot, two-wire configuration directly with the PT1000 without any method of wire compensation. A T_{WER} of 0.26°C for the PT100, however, is comparable with the ±0.3°C tolerance and therefore represents an unacceptable level of error for most precision applications. This example demonstrates the advantage of higher-resistance PRTDs in a two-wire circuit.

ERROR DUE TO PRTD SELF-HEATING

Another source of error for PRTDs is the self-heating of the RTD element as the excitation current flows through it. Excitation current flowing through the RTD resistance produces the voltage that you need to measure. This current should be as high as practical to ensure that the output voltage remains higher than the ADC's voltage-noise level. At the same time, the excitation current generates a power loss that warms the temperature sensor, thereby increasing the RTD resistance above the level it would otherwise assume due to the temperature you are measuring. You can calculate this thermal error due to RTD power dissipation from the package's thermal resistance, which you can obtain from the manufacturer's data sheet. The thermal error due to self-heating is a function of the current, as the following **equation** shows:

$$T_{TERR}=I_{EXT}^2\times R_T\times K_{TPACK},$$

where T_{TERR} is the thermal error due to self-heating in degrees Celsius, I_{EXT} is the excitation current through the resistive sensing element, R_T is the PRTD resistance at the current temperature T_C in degrees Celsius, and K_{TPACK} is the self-heating error coefficient: 0.7°C/mW.

For a circuit such as the one in **Figure 2**, you determine an optimal value of current-limiting resistor R_A using the above **equation** for T_{ERR}, plus a reference voltage you use in the measurement system—3V, in this case. **Table 3** lists R_A values for the 100Ω PTS1206 and the 1000Ω PTS1206. Using an R_A of 8.2 kΩ for the 100Ω PTS1206 and 27 kΩ for the 1000Ω PTS1206, the maximum thermal error ranges from 0.025 to 0.029°C, an order of magnitude less than the Class F0.3 tolerance of ±0.3°C. It is evident that the average excitation currents are stable and predictable over the temperature ranges in **Table 3**.

Another conclusion that you can draw from **Table 3** is that the maximum excitation currents dramatically differ from those of the 100 and 1000Ω R_T models. The excitation currents for the 1000 and 100Ω units are 108 and 362.4 µA, respectively. Thus, 1000Ω is preferable for low-power portable instrumentation. Its excitation current is less than one-third that of the 100Ω unit. R_A resistors should be metal-film types with ±0.1% or better tolerances, at least 0.25W power ratings,

and low temperature coefficients. To ensure that the resistors deliver the desired characteristics, you should acquire them from a reputable source such as Panasonic (www.panasonic.com), Rohm (www.rohm.com), or Vishay.

LINEARITY ERROR OF PRTD

PRTDs are nearly linear devices. Depending on the temperature range and other criteria, you can make a linear approximation by calculating the PRTD-resistance change over a temperature range of –20 to +100°C, as the following **equation** shows:

$$R(t) \simeq R(0)(1+T\times\alpha),$$

where R(t) is the PRTD resistance at t°C, R(0) is the PRTD resistance at 0°C, T is the PRTD temperature in degrees Celsius, and the constant α is 0.00385Ω/Ω/°C, according to IEC 60751. The constant α is a mean-temperature coefficient between 0 and 100°C. Using this **equation**, you can make a set of PRTD calculations (**Table 4**).

This **table**'s R_{RTD}1000 Linear column represents a linear approximation, according to the previous **equation**. The R_{RTD}1000 Nominal column lists the nominal PTS1206-1000 values according to manufacturing specification EN 60751:2008. The values in the Linearization Error column for the stated temperature range are all within the range of ±0.15%, which is better than the Class F0.3 tolerance of ±0.3°C for PTS1206.

Practical measurements per **Table 4** using a delta-sigma ADC confirm that digital representations of the temperature-reading errors remain within the limits for Class F0.3 tolerance. For wider range and higher accuracy, the temperature-measurement PRTD standard EN 60751:2008 defines the

TABLE 3 THERMAL-ERROR-CALCULATION BUDGET

V_{REF} (V)	K_{TPACK} (°C/mW)	T_C (°C)	100Ω R_T (Ω)	1000Ω R_T (Ω)	100Ω R_A (Ω)	1000Ω R_A (Ω)	T_{ERR} at 100Ω (°C)	T_{ERR} at 1000Ω (°C)	I_{EXT} at 100Ω (µA)	I_{EXT} at 1000Ω (µA)	V_{RT} at 100Ω (mV)	V_{RT} at 1000Ω (mV)
3	0.7	–55	78.3	783.2	8200	27,000	0.015	0.013	362.4	108	28.4	84.6
3	0.7	0	100	1000	8200	27,000	0.019	0.016	361.4	107.1	36.1	107.1
3	0.7	20	107.8	1077.9	8200	27,000	0.02	0.018	361.1	106.8	38.9	115.2
3	0.7	155	159.2	1591.9	8200	27,000	0.029	0.025	358.9	104.9	57.1	167

TABLE 4 PRTD CALCULATIONS FOR –20 TO +100°C

α (Ω/Ω/°C)	Temperature (°C)	Linear R_{RTD} of 1000Ω PRTD (Ω)	Nominal R_{RTD} of 1000Ω PRTD (Ω)	R_A (Ω)	V_{REF} (V)	V_{RTD} (V)	ADC code (LSB)	Error (%)
0.0035	–20	923	921.6	27,000	3	0.0991656	277286	0.15
0.0035	–10	961.5	960.9	27,000	3	0.1031597	288454	0.06
0.0035	0	1000	1000	27,000	3	0.1071429	299592	0
0.0035	10	1038.5	1039	27,000	3	0.1111151	310699	–0.05
0.0035	20	1077	1077.9	27,000	3	0.1150764	321776	–0.08
0.0035	30	1115.5	1116.7	27,000	3	0.1190269	332822	–0.11
0.0035	40	1154	1155.4	27,000	3	0.1229665	343838	–0.12
0.0035	50	1192.5	1194	27,000	3	0.1268955	354824	–0.13
0.0035	60	1231	1232.4	27,000	3	0.1308136	365780	–0.11
0.0035	100	1385	1385	27,000	3	0.1463801	409308	0

TABLE 5 TEMPERATURE-MEASUREMENT RESOLUTION

V_{REF} (V)	T_C (°C)	R_T at 100Ω (Ω)	R_T at 1000Ω (Ω)	R_A at 100Ω (Ω)	R_A at 1000Ω (Ω)	R_{TLSB} at 100Ω (°C/LSB)	R_{TLSB} at 1000Ω (°C/LSB)	R_{TNFR} at 100Ω (°C/NFR)	R_{TNFR} at 1000Ω (°C/NFR)
3	–55	78.32	783.19	8200	27,000				
3	0	100	1000	8200	27,000	0.00317	0.000926	0.021	0.0073
3	20	107.79	1077.9	8200	27,000				
3	155	159.19	1591.91	8200	27,000				

TABLE 6 TEMPERATURE-MEASUREMENT RANGE FOR ADC IN FIGURE 6

T_C (°C)	PRTD100 V_{RT} (mV)	PRTD1000 V_{RT} (mV)
–55	28.4	84.6
0	36.1	107.1
20	38.9	115.2
155	57.1	167
210	28.75	82.46

Notes:
Noise-free codes=(V_{MAX}–V_{MIN})/input-referred noise.
Noise-free codes=82.46 mV/2.86 µV p-p.
Noise-free codes=28,822 codes.
Temperature accuracy=210°C/28.82K.
Temperature accuracy=0.007°C.

behavior of platinum resistance versus temperature by the nonlinear mathematical Callendar-Van Dusen Equation.

For temperatures of 0 to 859°C, the linearization **equation** requires that you use two coefficients:

$$R(t)=R(0)(1+A\times t+B\times t^2).$$

For temperatures of –200 to 0°C, you add terms to that **equation**, which yields the following **equation**:

$$R(t)=R(0)[1+A\times t+B\times t^2+(t-100)C\times t^3],$$

where R(t) is the PRTD resistance at t°C, R(0) is the PRTD resistance at 0°C, and t is the PRTD temperature in degrees Celsius. You derive the A, B, and C calibration coefficients from measurements by RTD manufacturers, as specified by IEC 60751. A is 3.9083×10^{-3}°C–1, B is -5.775×10^{-7}°C–2, and C is -4.183×10^{-12}°C–4.

The first **equation** for R(t), on page 44, shows that nonlinearity errors increase for temperatures outside the band of 0 to 200°C (**Figure 4**). Using the second **equation** for R(t), in the first column of this page, reduces the error to negligible levels, except at low temperatures.

You can enlarge a portion of **Figure 4** over a narrower temperature range (**Figure 5**). The errors within a smaller range of –20 to +100°C, when using the first **equation**, for R(t), on page 44, are within ±0.15%. These errors become nearly negligible when you use the second **equation** for R(t), in the first column on this page. Precision measurements over a wider temperature range of –200 to +800°C require the implementation of these linearization algorithms using these two **equations**.

DELTA-SIGMA ADC MEASUREMENT RESOLUTION

These measurements require a low-power, 24-bit delta-sigma ADC with wide dynamic range and a high number of noise-free bits. Using such an ADC, you can calculate the resolution in temperature for the **Figure 2** circuit using the following two **equations**:

$$R_{TLSB}=\frac{V_{REF}\times(T_{CMAX}-T_{CMIN})}{FS\times(V_{TRMAX}-V_{RTMIN})};$$

$$R_{TNFR}=\frac{V_{REF}\times(T_{CMAX}-T_{CMIN})}{NFR\times(V_{TRMAX}-V_{RTMIN})},$$

where R_{TLSB} is the PRTD resolution at 1 LSB (least-significant bit), R_{TNFR} is the PRTD's NFR (noise-free resolution), V_{REF} is the reference voltage, T_{CMAX} is the maximum measurement temperature, T_{CMIN} is the minimum measurement temperature, V_{RTMAX} is the PRTD's voltage drop at the maximum measurement temperature, V_{RTMIN} is the PRTD's

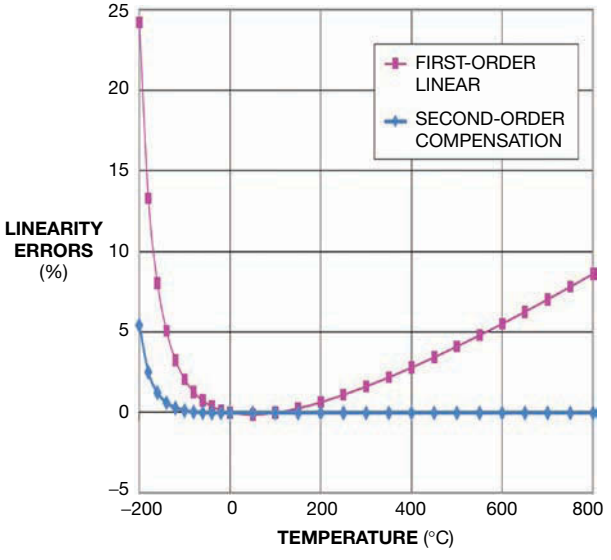

Figure 4 Nonlinearity errors increase for temperatures outside 0 to 200°C (pink curve). The errors decrease to negligible levels except at very low temperatures (blue curve).

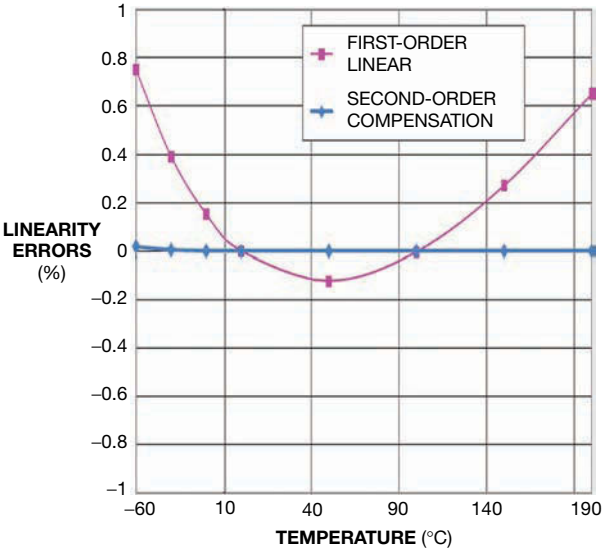

Figure 5 An amplified view of Figure 4 shows the area where the two graphs intersect.

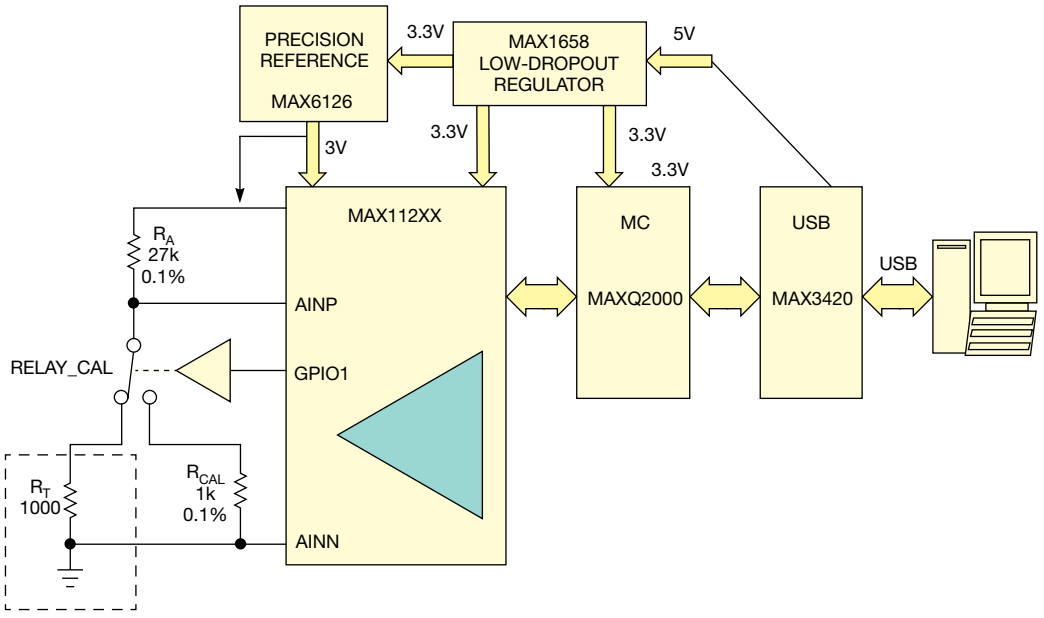

Figure 6 The precision data-acquisition system for measurements employs a delta-sigma ADC and includes a provision for simple calibration and computer-generated linearization.

voltage drop at the minimum measurement temperature, FS is the ADC's full-scale code for the IC in a single-ended configuration, and NFR is the ADC's noise-free resolution for the IC in the single-ended configuration.

You can tabulate the measurement resolution from the previous **equations** for R(t) for the 100 and 1000Ω PTS1206 (**Table 5**). The **table** provides the calculated values of degrees Celsius/LSB error and degrees Celsius/NFR error for a temperature range of –55 to +155°C. NFR represents the minimum temperature value that the ADC can differentiate. A 1000Ω R_{TNFR} of 0.007°C/NFR easily allows a temperature resolution of better than 0.05°C within the given range. This resolution is sufficient for most industrial and medical applications.

Another way to consider the ADC requirement for this application is to look at the expected voltage levels for different temperature points (**Table 6**). The last two rows show the range of differential voltage output for 100 and 1000Ω PRTD devices, respectively, and the notes below calculate how many noise-free codes the MAX11200 ADC produces. Note that the total range of output signal in PRTD applications is approximately 82 mV. The IC has input-referred noise of 570 nV at 10 samples/sec, which gives the application an NFR of 0.007°C over a 210°C span.

You can use a general-purpose output pin on the ADC to control the relay calibration switch. This action selects either the fixed R_{CAL} resistor or the PRTD (**Figure 6**). This versatility improves system precision and reduces the required calculations to those for the initial values of R_A and R_T.

In recent years, the decline in PRTD price and package size has made these devices desirable for a variety of precision temperature-sensing applications. Such applications require a low-noise ADC if you want to directly connect the ADC and surface-mount PRTD. Together, the PRTD and a delta-sigma ADC provide a temperature-measurement system that's ideal for portable sensing applications. Less wiring and lower thermal errors reduce the system complexity and cost, allowing you to implement a two-wire interface for distances as long as 2m. EDN

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AUTHORS' BIOGRAPHIES

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The realities of the maximum-supply-current specification for op amps

UNDERSTAND WHAT THIS COMMON, IMPORTANT PARAMETER REALLY MEANS AND WHY IT MAY BE MUCH HIGHER THAN YOU SEE ON THE DATA SHEET.

Most ICs' data sheets list a maximum supply current, but manufacturers often overlook the measurement conditions. For some rail-to-rail-output op amps, certain operating conditions can result in supply currents two to 10 times higher than the stated maximum. This article examines what to look for when trying to determine whether maximum supply current should be a concern for ICs—whether bipolar or CMOS.

Almost all IC data sheets have a guaranteed maximum supply current, but you cannot always use this number for your worst-case power calculations. It's well-known that CMOS digital parts have supply currents that increase as clock frequency increases, but what about analog parts, specifically op amps? You cannot always use the supply current plus the current to the load as a maximum.

Op amps operate in closed-loop mode, whereas comparators operate in open-loop mode. Designers seldom think about the ramifications of violating this given fact. A problem frequently arises, however, when you attempt to operate an op amp as a comparator. The approach is tempting because many op amps have low offset and low noise, so designers often press them into service as precision comparators. This scenario worked somewhat when older op amps operated from ±15V of power, and their input signals were within ±10V, especially if the designer had added some positive hysteresis to avoid oscillations and speed the transition through the uncertain region. The problem became serious with the advent of rail-to-rail-output op amps (**Reference 1**).

HISTORY

In the digital world, NAND gates, NOR gates, and other digital functions have distinctive military and ANSI symbols. However, in the analog world, op amps and comparators appear as triangles with two inputs and one output. Op amps have long found use as comparators, and many articles about both comparators and op amps as comparators appear in the literature. For example, as far back as 1967, when National Semiconductor (www.national.com) introduced the LM101A, the data sheet showed an application circuit using it as a comparator. Analog Devices' (www.analog.com) MT-083 data sheet provides a general discussion of comparators, covering how manufacturers specify them and the need for hysteresis, but it does not discuss using op amps as comparators (**Reference 2**). Another article discusses the general considerations when using op amps as comparators but does not discuss rail-to-rail-output op amps (**Reference 3**). The article does warn about the input differences with respect to common-mode input voltage and touches on the differences in differential-mode voltages.

Two different authors of an Analog Devices application note and tutorial advise against using an op amp as a comparator but then go on to conclude that doing so may be a proper engineering decision in some applications (**references 4** and **5**). According to another author, "the devil is in the details," and he does an excellent job of covering input-protection diodes, phase reversal, and several other op-amp characteristics but argues that careful attention to these details can pay off (**Reference 6**). He briefly mentions rail-to-rail-output op amps but not supply current.

As supply voltages decreased, one of the methods engineers used to maintain a large voltage swing was to convert the classic output stage to a rail-to-rail-output stage. **Figure 1** shows a classic output stage. Referring to the non-rail-to-rail output, the output can get only within approximately 1V of the positive supply. To get closer to the rails, engineers

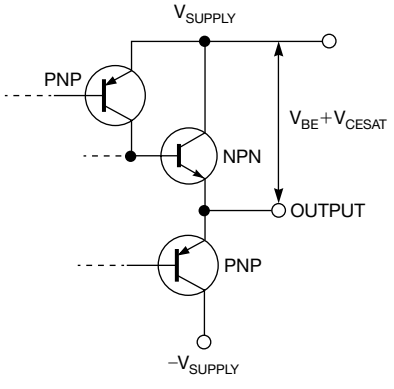

Figure 1 In a classic output stage, referring to the non-rail-to-rail output, the output can get only within approximately 1V of the positive supply.

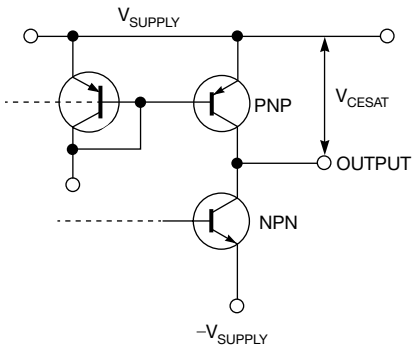

Figure 2 To get closer to the rails, engineers changed the output-stage transistors to a common-emitter configuration.

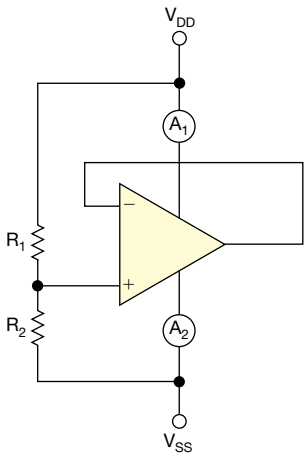

Figure 3 In the classic method for measuring supply current, the ammeters connect as shown to exclude the supply current of the resistive divider.

changed the output-stage transistors to a common-emitter configuration (**Figure 2**). The so-called rail-to-rail output can get within 50 to 100 mV of the supply, depending on the size of the output transistor and the load current.

Comparing these two output stages, note that the classic output stage has current gain but also has a voltage gain of less than one and a low output impedance. The rail-to-rail-output stage is a common-emitter stage and thus has voltage gain of approximately transconductance times the load resistance, R_L. R_L comprises the external load and the output impedance of the transistor. With the output operating more than several hundred millivolts away from the rail, output impedance is large and you can usually neglect it, but *not* if the output is close to the rail. Also note that you can consider the output as a classic two-transistor current mirror, which turns out to be the crux of the problem.

In normal operation, the middle stage pulls down the base-collector node, driving more current into the load and raising the voltage. With negative feedback, as the output voltage rises, the input and middle stages reduce the drive until the closed loop is balanced.

When you use an op amp as a comparator, the middle stage pulls down the base-collector node, trying to close the loop. With no feedback, however, it continues to pull harder and harder. This additional current finds a path from the positive-supply pin to the negative-supply pin and appears as additional supply current. You can drive the output stage in several ways, and combining the difference in mobility between holes and electrons, the increase in supply current is usually asymmetrical.

A HANDS-ON TEST

A comparison of a bipolar op amp and a CMOS op amp from Analog Devices and three of its major analog competitors quantifies this effect (**Table 1**). The comparison includes National Semiconductor's venerable, non-rail-to-rail-output LM358 dual op amp and LM393 dual comparator. The tests measure the supply current as a function of supply voltage using three circuits.

Figure 3 shows the classic method for measuring supply current. The ammeters connect as the **figure** shows to exclude the supply current of the resistive divider. Two ammeters verify that the supply current is accurate and excludes any undesired current path through the input pins. The resistor values are noncritical and ensure that the input to the op amp is within the specified input-voltage range from the data sheet.

TABLE 1 BIPOLAR AND CMOS OP-AMP COMPARISON

Part Number	Type	Voltage (V)	Spec (mA)	Follower (mA)	V_{OL} (mA)	V_{OH} (mA)
LM358	Bipolar	30	2	0.707	0.506	0.671
LM393	Bipolar	36	2.5	0.548	0.565	0.567
OP184	Bipolar	30	2	1.239	1.188	6.683
A	Bipolar	24	0.45	0.361	3.442	0.708
B	Bipolar	30	3.4	2.785	2.051	3.998
C	Bipolar	30	4.5	4.063	5.336	3.786
AD8605	CMOS	5	1.2	0.998	0.544	0.625
A	CMOS	5	0.9	0.511	0.361	10.152
B	CMOS	5	2.4	1.916	2.759	2.475
C	CMOS	5	1.4	1.039	0.822	0.667

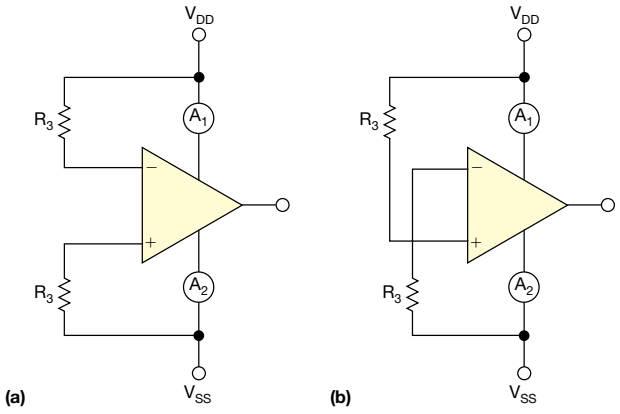

Figure 4 Another method allows for measurement of supply current when the circuit is operating in open-loop mode: with a low output (a) or a high output (b).

To measure supply current when the circuit is operating in open-loop mode, such as operation as a comparator, another method is used (**Figure 4**). Some low-noise, bipolar op amps have diodes between the inputs to protect the differential input pair, so the data sheet lists the maximum differential voltage in the absolute-maximum table as ±0.7V. Any internal series resistors usually have values of 500Ω to 2 kΩ.

The absolute-maximum table may state that the maximum differential voltage is plus or minus the supply voltage, but this specification does not mean that the part operates. You should consult a simplified internal schematic. If you don't find one in the data sheet, call the manufacturer to obtain it.

In these two configurations, the choice of resistor values is more critical. The resistor values should be low enough to cause the differential input voltage to be at least 0.5V to guarantee that the output drives hard into the rail but high enough to cause no damage to the internal diodes. The chosen values limit the input current to less than 1 mA.

BIPOLAR RAIL-TO-RAIL OP AMPS

All of the bipolar rail-to-rail-output op amps have supply current greater than the maximum op-amp supply current in one or both comparator circuits. You can drive the output stage in several ways, and some methods result in a supply-current increase when driving to one rail or the other. For Texas Instruments' (www.ti.com) OP284, the data sheet shows a simplified schematic of the second and output stages (**Figure 5**).

If Q_5, Q_3, and Q_4 drive the output voltage high, the supply current will be a function of the values of R_4 and R_6. You select these values to maximize the op amp's performance and minimize die area, not to enhance comparator operation. When Q_6, R_1, and Q_1 drive the output voltage low, R_1 will determine the supply current. Again, select the values of R_1, I_1, and other components for op-amp performance, not comparator performance.

CMOS RAIL-TO-RAIL OP AMPS

CMOS op amps have interesting behavior. In some cases, the supply current decreases when you drive it to a rail. The output stage of a CMOS op amp comprises common-source PMOS and NMOS transistors, and gain enters during the output stage. The gain is the transconductance times the load resistance. You can get a reasonable value of transconductance because the drive circuit sets the quiescent current to a certain value.

As the output drives into the rail, the drive circuit decreases the drive on the complementary transistor. Depending on the transfer characteristics from the top transistor to the bottom transistor, the current decreases. Note the wide variation in behavior among the four CMOS op amps.

To reduce die size and, therefore, cost, both op amps can share some circuits, such as bias circuits and the associated start-up circuit. If one op amp operates outside its normal range and causes the bias circuit to malfunction, then the other op amp will also malfunction (**Reference 7**). For battery-operated systems or when using low-current series regulators, you must consider the additional supply current. Battery life may be less than you calculate, or the regulator may not start up under all conditions, especially over temperature.

THE ABSOLUTE-MAXIMUM TABLE MAY STATE THAT MAXIMUM DIFFERENTIAL VOLTAGE IS PLUS OR MINUS THE SUPPLY VOLTAGE, BUT THIS SPECIFICATION DOES NOT MEAN THAT THE PART OPERATES.

For new designs, the easiest approach is to avoid using op amps as comparators. If you must use one as a comparator, then you should check the data sheet to see whether the manufacturer has any information on the device's operation

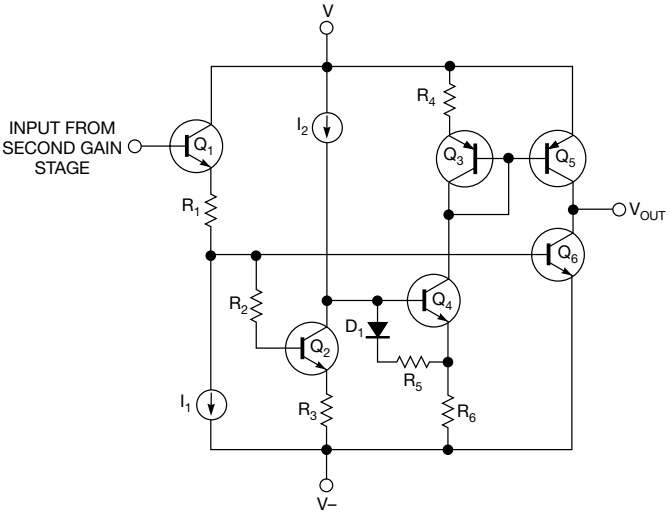

Figure 5 In the OP284, if Q_5, Q_3, and Q_4 drive the output voltage high, the supply current will be a function of the values of R_4 and R_6. You select these values to maximize the op amp's performance and minimize die area, not to enhance comparator operation.

as a comparator. Some manufacturers include this information (**Reference 8**). If the data sheet omits this information, ask the manufacturer for it. If the manufacturer cannot provide it, measure several date codes yourself using the circuits in the **figures** and add 50% for a safety factor.

Rail-to-rail-output op amps have unique characteristics when you operate them as comparators. The best ways to improve battery life and increase performance are to use a low-cost comparator when your design requires a comparator, to tie off any used op-amp sections as followers and connecting the noninverting input to a stable voltage within the input-voltage range of the op amp, and to use singles and duals as appropriate instead of quads.

Supply current may greatly exceed the maximum that the data sheet states. Under carefully considered conditions, you can use unused op amps as comparators, but using the proper mix of op amps and comparators will result in lower supply current and well-defined performance. EDN

ACKNOWLEDGMENT

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AUTHOR'S BIOGRAPHY

Harry Holt has been a staff applications engineer in the precision-amplifier group at Analog Devices Inc (San Jose, CA) for four years. Previously, he spent 27 years in both field and factory applications at National Semiconductor for a variety of products, including data converters, operational amplifiers, references, audio codecs, and FPGAs. Holt has a bachelor's degree in electrical engineering from San Jose State University (San Jose, CA) and is a life member of Tau Beta Pi and a senior member of the IEEE.

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READERS SOLVE DESIGN PROBLEMS

Circuit provides universal ac-input-voltage adapter

JB Castro-Miguens, Cesinel, Madrid, Spain, and
C Castro-Miguens, University of Vigo, Vigo, Spain

The input-rectifier stage of an offline power supply converts an ac-line voltage to a dc voltage, which powers a dc/dc converter. If you configure the rectifier section as a full-wave bridge for a universal mains input of 92 to 276V rms and 47 to 63 Hz, you must design the dc/dc converter to operate over a wide range of input voltages. This approach increases the cost of components and reduces the efficiency of the dc/dc converter.

For 115V-rms operation, if you configure the rectifier stage as a simple bridge, the output-voltage ripple ranges from 113 to 192V, given a ±20% tolerance on the ac input voltage (**Table 1**). Note that the voltage ripple corresponds to an effective output capacitance of 115 µF, the series equivalent of two 330-µF capacitors, and to a load of 250W. However, if you configure the rectifier stage as a voltage doubler for 115V-rms operation, the output voltage ranges from 200 to 372V—much closer to the 215 to 387V voltage ripple for 230V-rms operation.

This Design Idea proposes a rectifier stage that automatically configures itself as a voltage doubler for 115V-rms±20% line operation. **Figures 1** and **2** show the proposed rectifier stage. The STMicroelectronics (www.st.com) snubberless BTB16-600BW TRIAC (triode alternating current) is suitable for a 250W load (**Figure 1**).

For 115V-rms±20% line operation, the Reference terminal of the TL431 programmable shunt regulator has a voltage lower than its 2.5V internal reference (**Figure 2**). In this situation, the MOSFET is on, and the IL4216 optocoupler continuously fires the TRIAC.

For 230V-rms±20% line operation, the Reference terminal has a voltage higher than 2.5V, and the MOSFET and the TRIAC are off. C_1 is necessary to prevent the rectifier from starting in doubler mode when you turn on the supply with a low rectified line voltage.

This approach prevents the rectifier stage from changing from doubler mode to bridge mode during start-up, which would create a voltage drop in the bulk output capacitors that would differ from the voltage in steady-state operation. This difference would cause one of the capacitors to have an abnormally

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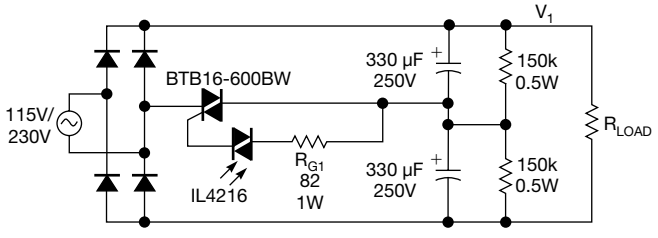

Figure 1 This ac-rectification circuit uses a TRIAC and an optocoupler to automatically switch between doubler and bridge configurations.

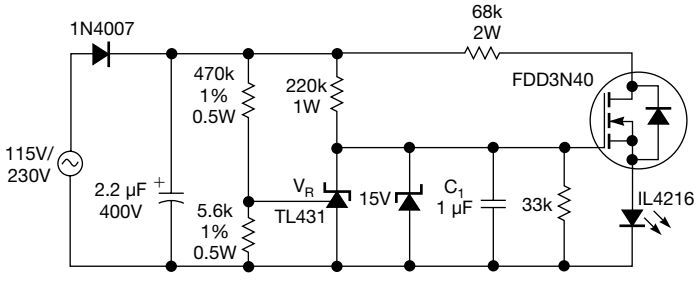

Figure 2 This control circuit uses a programmable shunt-regulator IC to sense the ac-input-voltage range.

high voltage and the other to have an abnormally low voltage.

A practical value of C_1 is 1 µF, which introduces an approximately 8-msec time delay for starting in doubler mode. You can use a 15V zener diode to clamp the gate voltage of the MOSFET. EDN

TABLE 1 200W INPUT-RECTIFIER/FILTER SECTION

	115V-rms±20% 60-Hz bridge	115V-rms±20% 60-Hz doubler	230V-rms±20% 50-Hz bridge
RMS ac-line voltage	92 to 138	92 to 138	184 to 276
Peak ac-line voltage	130 to 195	130 to 195	260 to 390
V_{1MIN}–V_{1MAX}	113 to 192	200 to 372	215 to 387

Logic probe uses two comparators

Vladimir Rentyuk, Zaporozhye, Ukraine

Measurement instruments must not affect the circuits they're measuring. A logic probe, for example, must correctly detect logic levels, and it must place no undue loads on the test circuit. The logic probe must set thresholds on automatically checking logic levels, depending on the supply voltages of the ICs it is checking. It should also not cause the checking circuit to function incorrectly.

The logic probe in a previous Design Idea suffers from loading problems (**Reference 1**). Its thresholds do not adequately depend on the supply voltages of the ICs it is checking. After some analysis, you'll find that the circuit can have an input-current range of 50 to 80 µA. Unfortunately, CMOS ICs such as NXP's (www.nxp.com) HCMOS 74HC/HCT/HCU (**Reference 2**) and Signetics' (www.signetics.com) LOCMOS HE4000 families have input current as low as ±1 µA. The HE4000 family of logic ICs has input currents of ±0.1 to ±0.3 µA. Connecting the referenced logic probe to input pins of these ICs loads the circuit under test and distorts the waveforms to the point at which you may not be able to see some problems, such as glitches, on an oscilloscope. Logic probes also have negligible input capacitance. Too much capacitance attenuates at high frequencies.

The circuit in **Figure 1** is an alternative logic probe for ICs of the 74HCxx family, for example. It comprises comparators IC_{1A} and IC_{1B}. Not every comparator will work properly in this circuit. The comparator must, for example, operate with minimal supply voltages, and it must have low input leakage current. The Analog Devices (www.analog.com) AD823AR or an equivalent comparator is a good choice.

Comparators IC_{1A} and IC_{1B} check logic-high and -low levels, respectively. The resistor-divider network comprising the 1%-tolerant, surface-mount, size-0805 R_4, R_5, and R_6 resistors sets the voltage levels, which vary in relation to the power-supply voltage. Connect the probe circuit to the same power supply that you use to power the circuit under test, allowing the comparator voltages to track the circuit's power supply. Green LED_1 and red LED_2 indicate logic-high and -low levels, respectively. If the input voltage is between those levels, neither LED will illuminate. **Table 1** highlights the logic-level voltages for the 74HCxx family of ICs, and **Table 2** shows the voltage levels for the 4000 series ICs.

The input current of the AD823AR is less than ±3 µA at a drain-to-drain voltage of 5V, ±6 µA at a drain-to-drain voltage of 10V, and ±9 µA at a drain-to-drain voltage of 15V. You can reduce this current by increasing the value of

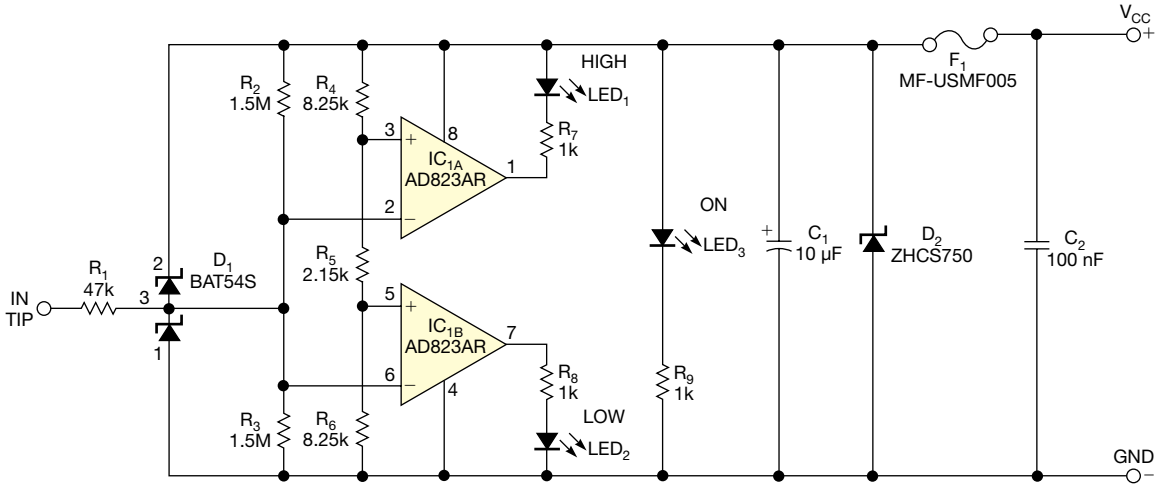

Figure 1 Two comparators and a resistor network track power-supply voltages and set logic-voltage levels.

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TABLE 1 LOGIC-LEVEL VOLTAGES FOR 74HCXX FAMILY

Parameter	Symbol	Value (V)	Threshold (V)	Value (V)	Threshold (V)
DC-supply voltage	V_{CC}	4.5		6	
Low-level input voltage	V_{IL}	2.1	1.99	2.8	2.65
High-level input voltage	V_{IH}	2.4	2.51	3.2	3.35

Note: Thresholds were chosen on the basis of typical logical levels for ICs in the 74HCxx family.

TABLE 2 LOGIC-LEVEL VOLTAGES FOR 4000 FAMILY

Parameter	Symbol	Value (V)	Threshold (V)	Value (V)	Threshold (V)	Value (V)	Threshold (V)
DC-supply voltage	V_{CC}	5		10		15	
Low-level input voltage	V_{ILMAX}	1	0.93	2	1.86	2.5	2.51
High-level input voltage	V_{IHMIN}	4	4.3	8	8.61	12.5 8.25	11.62

Note: R_4, R_5, and R_6 are 6.2, 30, and 8.25 kΩ, respectively.

resistors R_2 and R_3, which are 1.5 MΩ in **Figure 1**.

The network comprising R_1 and D_1, two BAT54S Schottky diodes, protects the logic-probe circuit from overvoltage at its input, from ESD (electrostatic discharge), and from signals of negative polarity. Yellow LED_3 indicates when the logic-probe circuit and the circuit under test start up. The yellow LED is useful if you connect the probe to the circuit under test with crocodile clips. This approach ensures that both the probe and the test circuit are always on. D_2 and resettable fuse F_1, an MF-USMF005, which has a hold current of 0.05A and which comes in a surface-mount package, protect the probe circuit from improperly powering up. Tantalum capacitor C_1, in size A or B, and ceramic capacitor C_2, in size 0805, prevent the test circuit from influencing power for the logic probe. R_1 minimizes the influence of input capacitance on this logic probe.

The logic-level thresholds automatically depend on the supply voltages (**tables 1** and **2**). You can use this logic probe with other ICs, such as the 74HCU, 74HCT, or 4000 series. You can freely select the value of R_6. You can also calculate the value of R_5 and R_4 using $R_5=V_H/(V_L/R_6)-R_6$ and $R_4=V_{DD}//(V_L/R_6)-R_6-R_5$, where V_{DD} is the supply voltage of the device, V_H is the threshold for checking the high logic level for the chosen supply voltage, and V_L is the threshold for checking the low logic level for the chosen supply voltage. EDN

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DAC fine-tunes reference output

Fons Janssen, Maxim Integrated Products, Bilthoven, Netherlands

Data converters must have a stable reference voltage to accurately measure or generate analog signals. Such references offer many guaranteed levels of precision and stability. Their variety of output-voltage levels is much smaller, which manufacturers specify as standard values, such as 2.048, 2.500, or 4.096V. You sometimes need to dynamically calibrate the reference, fine-tune its output value, or generate a slightly different value. For instance, when you measure a voltage with a resistive divider, you could adjust the reference voltage to compensate for an error in the divider.

You can adjust any three-terminal voltage reference using a resistor, a current sink/source, and a buffer amplifier (**Figure 1**). Sinking or sourcing current causes the resulting voltage drop across R_1 to subtract from or add

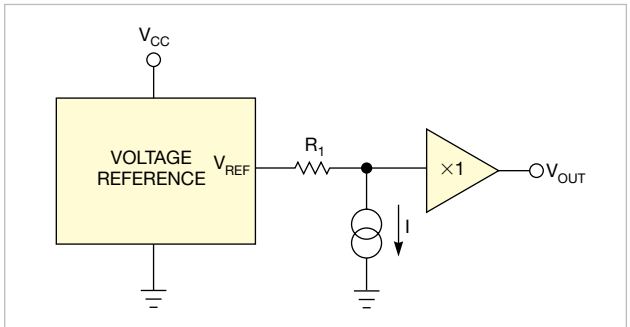

Figure 1 Adding a resistor, a current source, and a buffer to a voltage reference lets you adjust its output.

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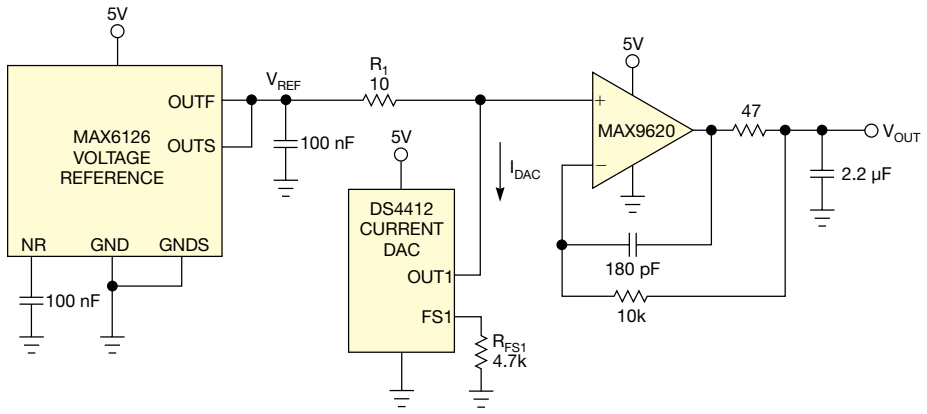

Figure 2 You can implement the idea of Figure 1 with three ICs.

to the nominal reference output, V_{REF}:

$$V_{OUT}=V_{REF}-I\times R_1.$$

The buffer amplifier isolates V_{OUT} from the load, so the only current flowing through R_1 is that from the current source. You can implement this idea with a highly stable voltage reference, a current DAC, and a low-offset op amp (**Figure 2**). If you choose a value of 4.7 kΩ for R_{FS1}, the full-scale DAC current is 0.981 mA, as the data sheet states. With a value of 10Ω for R_1, this current value yields a tuning range of ±0.981 mA×10Ω=±9.81 mV, divided into 31 steps of 0.654 mV each.

Depending on the performance grade of the reference and its package, the initial output accuracy can be as high as ±0.02%. The DAC's output-current accuracy is only ±6%, but the tuning range is small, so the large tolerance has only a small effect on the output error. Combining these values with a 1% resistor tolerance for R_1 and the maximum offset value for the op amp yields the following **equation** for the maximum initial output-voltage error:

$$0.0002\times V_{REF}+\sqrt{0.06^2+0.01^2}\times|I_{DAC}|\times R_1+V_{OFFSET}.$$

If you use a 2.048V reference, the following **equation** calculates the error:

$$0.4096\ \text{mV}+0.5969\ \text{mV}\times\frac{|\text{DAC}|}{15}+10\ \mu\text{V},$$

where DAC represents the DAC's decimal equivalent-output value (−15≤DAC≤15). Thus, the DAC introduces a maximum error of 0.5969 mV, yielding a total of roughly 1 mV when you combine it with the initial accuracy of the voltage reference itself.

Because the DAC has an operating-temperature range of −40 to +85°C, you use the voltage reference's drift specification in that same range, ±3 ppm/°C. IC makers often use the box method to specify temperature drift (**Reference 1**). You can then calculate this maximum reference-voltage drift over the temperature range of −40 to +85°C:

$$125°\text{C}\times\pm3\ \text{PPM/°C}\times2.048\text{V}=\pm0.768\ \text{mV}.$$

The drifts in the DAC, R_{FS1}, and of R_1 cause the drift in the second term ($I_{DAC}\times R_1$). The IC vendor specifies drift in the DAC as a typical value of ±75 ppm/°C. You assume ±25 ppm/°C for the resistors. These values yield a typical drift:

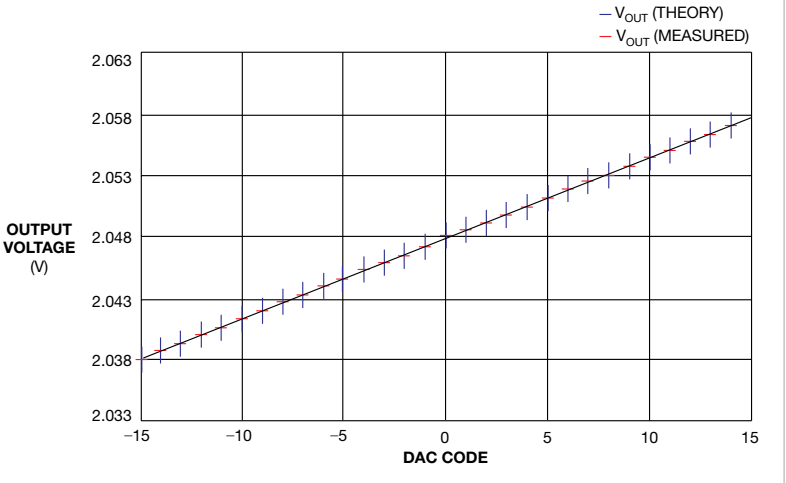

Figure 3 You can examine the theoretical (blue line) and measured (red bars) output voltage as a function of DAC code. The nominal reference output is 2.048V. Error bars show that the accuracy drops slightly toward the absolute higher values of DAC code. The graphic omits error bars for the voltage meter.

$$\sqrt{(125°C\times\pm75\ PPM/°C)^2+(125°C\times\pm25\ PPM/°C)^2+(125°C\times\pm25\ PPM/°C)^2}\times I_{DAC}\times R_1=\pm0.102\ mV\times\frac{DAC}{15}.$$

The DAC and the resistors typically introduce only roughly ±0.1 mV of drift, which is substantially lower than the maximum drift of the voltage reference. The IC vendor specifies the op amp's maximum input offset over temperature as 25 µV—also much lower than the maximum drift of the voltage reference. You can examine the DAC's output voltage as a function of its input code, using error bars to indicate the initial accuracy and temperature drift (**Figure 3**). The error increases slightly for the higher DAC values, mostly due to temperature drift. The measured values are at room temperature and are close to the theoretical values. EDN

REFERENCE

1 Fry, David, "Calculating the Error Budget in Precision Digital-to-Analog Converter (DAC) Applications," Application Note 4300, Maxim Integrated Products, Sept 25, 2008, http://bit.ly/rtE0TR.

LEDs indicate sound level

Stephen Kamichik, Ile Bizard, PQ, Canada

This Design Idea describes a battery-operated, portable sound-level meter (**Figure 1**). Its portability makes it useful for detecting the source of noise in automotive engines and power trains, factory machinery, and residential HVAC (heating/ventilation/air-conditioning) systems.

Resistor R_1 biases the condenser microphone. C_1 couples R_1 to transistor Q_1. Q_1 and R_2 through R_5 form a self-biasing common-emitter amplifier. Resistor R_5 provides negative feedback. Shunt capacitor C_2, in parallel with R_5, increases the amplifier's voltage gain. The input resistance of the amplifier is equal to $(R_2R_3)/(R_2+R_3)$.

In this circuit, the input resistance is 10.8 kΩ. Capacitor C_3 limits the high-frequency response of the amplifier. Capacitor C_5 is a filter capacitor. Capacitor C_4 couples the output of the amplifier to the load, P_1.

IC_1, a 5V positive-voltage regulator, regulates the 9V battery supply to 5V for IC_2, an LM3915 dot/bar-display driver. IC_2 senses analog voltage levels and drives LED_1 through LED_{10}.

In the sound-level-meter circuit, IC_2 provides a logarithmic 30-dB display. IC_2 also contains an adjustable voltage reference and an accurate 10-step voltage divider.

The high-impedance input buffer accepts signals from ground to within 1.5V of the positive supply. You set the sound-level meter to bar mode by connecting Pin 9 to Pin 3. Pin 3 is the V+ pin of IC_2 and connects to IC_1's Pin 3, which is the device's output voltage. Potentiometer P_1 functions as a sensitivity control. Resistor R_6 sets the voltage reference for IC_2. EDN

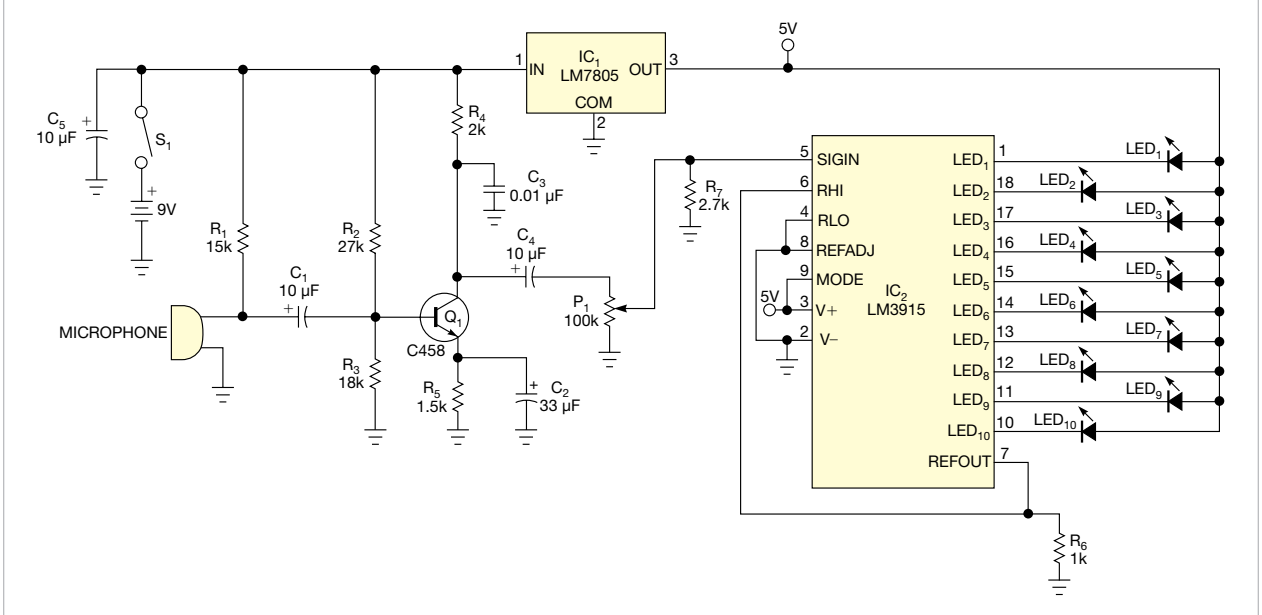

Figure 1 This sound-level meter uses an LM3915 LED driver.

productroundup

COOLING AND ENCLOSURES

Orion Fans' OA300ST series fan tray fits into standard 19-in. racks

The OA300ST series of ac three-position, short fan trays features three high-performance, sealed-ball-bearing fans for installation in any standard 19-in. rack. The fan trays fit applications in industrial-control cabinets and network-system enclosures. Available in 115 and 230V-ac versions, the fan trays achieve airflows as great as 320 cfm, and low-noise versions are available. The trays include a 2M-length power cord, a lighted rocker switch, and a resettable circuit breaker. The standard high-speed model has 45W power. Operating temperatures range from –20 to +80°C, and life expectancy is 60,000 hours at 40°C. OEM price for the OA300ST series is $125 (99).
Orion Fans, www.orionfans.com

ATS's iQ-200 instrument measures temperature, velocity, and pressure

The iQ-200 thermal-analysis system measures the temperatures of solid materials and the surrounding air, and it tracks air velocity and air pressure at multiple points to comprehensively profile heat sinks, components, and PCBs. The laboratory instrument simultaneously captures data from as many as 12 J-type thermocouples, 16 air-temperature/velocity sensors, and four differential-pressure sensors. It records temperature data from –40 to +750°C. As many as 16 of the vendor's low-profile candlestick sensors, which you can place throughout a system, measure air temperature and velocity. The device tracks air temperature from 20 to 65°C and measures air velocity from 0 to 6m/sec (1200 feet/minute). The differential transducers capture pressure-drop data along PCBs, assemblies, and orifice plates. Pressure measurements range from 0 to 0.15 psi. List price for the iQ-200 is $24,500, including 12 J-type thermocouples, 16 candlestick sensors, and four differential-pressure sensors.
Advanced Thermal Solutions, www.qats.com

Optical Cable's data-center cabinet offers durable, flexible options

This data-center cabinet features a 6.5-in.-deep rear power-distribution unit/cable section with room to attach power-distribution hardware and secure multiple cable connections. Angled cable entries and exits allow easy access, minimizing cable strain on power cords. The power-distribution units face outward, providing easy visibility to the operating power-distribution system. Users can reverse a swing on the front for easy access in any site. With 63% perforation on the front and rear doors, servers and switching hardware breathe easier and run cooler. The starting manufacturer's suggested retail price for the cabinet frame is $2340.45. Door, side-panel, roof, and nonstandard-color options are available.
Optical Cable Corp, www.occfiber.com

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DOUGLAS FORST • CMC INDUSTRIAL ELECTRONICS INC

Going against the grain dust

As the owner of an industrial-controls company, I frequently receive calls from customers. Recently, a representative from our best customer called, asking for help with a sensor on a monitoring system. The company happens to be in the same city as ours, so I was able to visit the site. Our company manufactures an intrinsically safe monitoring system for conveyors and other equipment in hazardous locations and other industrial and commercial facilities. The principle of intrinsic safety is to restrict the amount of available energy in the field wiring system to less than the amount that could cause an explosion or a fire.

This customer operates a grain elevator that has a high risk of fire and explosion from grain dust. Grain-dust explosions are responsible for a number of deaths each year worldwide. The customer's large installation uses approximately 2500 sensors on the network. Our system is designed to detect problems, such as hot bearings or off-track belts, with the conveying equipment. One of the customer's speed sensors was on a long belt, but the sensor was frequently failing after nearly a year in use.

When I reached the site, the electrician had already done most of what I would normally have done. Our speed sensor uses a magnetic code wheel triggering Hall-effect sensors to determine the speed of the belt. The customer's sensor would work fine until the code wheel began to turn. Then, for no apparent reason, the sensor stopped operating. The design includes a working and verified watchdog; whatever was interfering with the unit was strong enough to override all of the protection. The sensor would resume normal operation if an operator powered it off and back on again.

The electrician had more than once replaced the sensor, the controller communicating with the sensor, and even the junction box it connected to. Two temperature sensors that plugged into the same box worked fine. I repeated most of the electrician's work and even moved the sensor to another belt, where it worked perfectly.

I had heard a strange snapping sound when the conveyor was running and wanted to see what it was. The electrician said it was just grain falling or the belt splice, but I wasn't so sure. We started the belt, and, sure enough, as the belt reached speed, you could hear a loud, repeated snapping sound. The interval between snaps changed as the belt reached speed. The belt ran for about a minute before the control system stopped it due to an underspeed condition; the sensor had failed once again. As the belt slowed down, the snapping interval grew longer until the belt, and the snapping, stopped.

We again restarted the belt to determine the source of the noise: Inside the rigging of the conveyor, a half-inch-long, white-hot arc was jumping from a return roller to the frame of the conveyor and landing just a quarter-inch away from a pile of highly flammable grain dust. The roller and the belting material were rubbing together, creating static electricity and causing the arc, which could have destroyed a multimillion-dollar facility and killed or injured many people.

The electrician then remembered that this roller had been replaced just before the problem started. This roller was from a new supplier; it had thermoplastic end caps connecting the metal roller to the bearing shaft, effectively insulating the metal roller from the conveyor frame. The new roller had created the perfect Van de Graaff generator. All previous rollers had been of an all-metal construction that effectively grounded any static charge. Using some Category 5 cable, we rigged up a simple grounding wiper and restarted the conveyor. Everything worked perfectly. How the static discharge was getting into the sensor almost 10 feet away, I will never know. EDN

Douglas Forst is president of CMC Industrial Electronics Inc (Burnaby, BC, Canada).

DANIEL VASCONCELLOS

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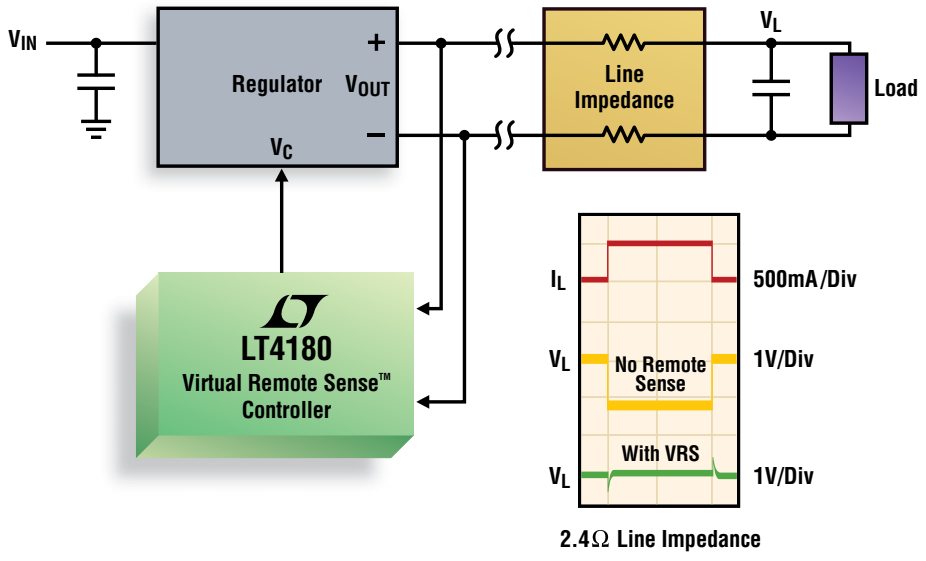

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